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Analysis of Efficient FPGA Based PID Controller for Dc-Dc Buck Boost Converter Using Hardware Co-Simulation Setup

Shafquat Hussain[1], Waqar Ahmed[1], Ahmed Muddassir Khan[1] Rizwan Ali[2]

Abstract:

Converters are widely used in smart grid applications where multilevel dc voltage sources are required in a system. The object of the paper is to design dual input DC-DC converter and implement FPGA based PID controller on that converter. There are few critical challenges in existing converters: low efficiency, slow response time, large circuit size due to more number of switches, and subsequently low PWM signal quality. Moreover, a separate converter is required for each source used. For the solution to this problem, a dual input DC-DC converter is proposed. In this work, we proposed and analyzed an efficient FPGA based PID controller using Hardware Co-simulation for DC-DC Buck-Boost Converter and compare their results. We have successfully integrated two different sources of energy, which are being fed to the power stage. The control of this converter topology is implemented by using FPGA kits Virtex5 and Virtex7. Furthermore, the efficiency of both kits is compared and analyzed. By comparison, the virtex7 has more slice register, LUTs, and occupied slices than virtex5. The proposed converter has high efficiency, fast response time, and compact size due to the least number of switches compared to the conventional topology of those converters.

Keywords: *Buck Boost converter, FPGA, PID Controller*

1. Introduction

Demands for Renewable Energy systems are exponentially increasing day by day to cope up with the challenges of high cost, pollution, and wastage in conventional energy sources. Moreover, system's flexibility, stability, and reliability can be enhanced using the integrated energy source like solar and wind. As renewable energies like solar and wind may not exist the whole day, their obtainability relies on their nature and weather conditions. If the load is supplied through multiple sources, the reliability of the system will be further improved. Similarly interest in the automobile industry shifted from fuel to the electric vehicles or Hybrid Electrical Vehicle (HEV)[1-4].

There are many topologies of the converter from literature, but two main topologies are isolated and non-isolated converter topologies. In the case of isolated topologies, the single binding and multi-binding transformers have high complexity, which will reduce the converter's efficiency and compactness. The non-isolated converter topology is preferred due to cost and efficiency issues. [5-6].

There are few generalized approaches for the development of Microcontroller Unit (MCU) which is the heart of any converter. By taking benefit of this ability, this paper proposes the

[1]Department of Electrical Engineering, FEST, Indus University, Karachi, Pakistan
[2]Department of Electronic Engineering, NED University of Engineering and Technology, Karachi, Pakistan
Corresponding Author: ahmed.muddassir@indus.edu.pk

different case scenarios and system behavior, and the desired simulating parameters can be determined and (MCU) Microcontroller unit [7]. A critical issue in using MCU is that there is a slow or delayed response subsequently output of converter will be effected.

To resolve this issue field-programmable gate array (FPGA) technology is employed which has much advanced to design intricate and fast dynamics control techniques and at the realistic operating frequency estimate the performance in the real-time foundation [8]. Moreover, FPGAs are flexible in implementation because desired logic is programmed through implementation the algorithms as per requirement of application and it can be esailly modified if required [9-10]. Hence, designing the converter based on FPGA, is more straightforward than modification process in MCU [11].

In FPGA programming, First Hardware description language (HDL) code is converted into binary after that, and it is uploaded to the FPGA kit with the help of the compiler. Any algorithm can be implemented on FPGA by first changing HDL code to binary code and finally uploading that binary code into the FPGA kit with a compiler's help. A programmer who uses the MATLAB program can easily convert MATLAB code into HDL code by using MATLAB. This approach produces logic faults because of its conversion to fixed data from floating-point [12]. Another more efficient technique is the Xilinx system generator (XSG), which consents the user to program multiple FPGA devices [13].

In [14] the proposed topology has been controlled through conventional PID controller in any MCU. While in this paper PID controller is implemented in FPGA which has high speed as compared to the conventional MCUs.

Other parts of the paper are: In part 2, the working of dual input DC-DC buck-boost converter is presented. In part 3, controller implementation is shown. In part 4, there are results and discussion that show the proposed converter's simulation results, and in part 5, the conclusion, in which achievement of proposed model is discussed

C_7 coordinate in case of 1st model Figure 9 correlates to C_3 in 2nd Model Figure 10 and have almost same values of equivalent resistivity and magnetic field intensities describer earlier.

C_7 coordinate in 2nd model Figure 10 and 3rd model Figure 11 has same results due to same configuration in case of 2nd model Figure 10 currents I_4 and I_5 are flowing from C_7 both of these currents are not similar and opposite to each other due to which some net current flows which is lesser than the current of C_7 in model no 1 and has a bit lesser magnetic field intensity and a bit higher equivalent resistivity than C_7 in model no 1

2. Working And Steady-State Analysis Of Dual Input Dc-Dc Converter

The circuit diagram of the proposed converter is shown in fig. 1. In the given topology, the switches like T1 and T2 are bidirectional conduction (B.C.) and bidirectional blocking (B.B.). The freewheeling current is provided by the diodes D1 and D2 as in fig. 2. The two energy sources are supplied to the converter, which involves two switches T3 and T4, with an inductor connected in series to eliminate the current ripples and a capacitor connected in parallel for removing voltage ripples from dual input DC-DC buck-boost converter.

The operation of switches T1 and T2 as On and off from which the converter can change its mode of operation. The capability of Buck-boost can be performed by switch T3, while the switch T4 performs the bidirectional operation. The two input dc voltage sources are V1 and V2, where V.O. and I.O. are the output voltage and load current, respectively.

2.1. Steady-State Analysis

Due to the different switching strategies of switches, various operating sequences are gained. The switching pattern will be chosen from the power utilization of sources. The methods of producing gate pulse namely;

a) Rising edge synchronization,

b) Falling edge synchronization and

c) Intermediate synchronization

Over a complete switching cycle, the switches will perform their duty cycle (D) mathematically

$$t_1 = (d_1 - d_2)Ts \quad (1)$$

$$t_2 = d_{12}Ts \quad (2)$$

$$t_3 = (d_2 - d_{12})Ts \quad (3)$$

$$t_4 = (1 - d_1 - d_2 + d_{12})Ts \quad (4)$$

Where,

d_1= duty cycle of switch T_1.

d_2 = duty ratio of switch T_2.

For the generation of gate pulses, the Intermediate synchronization technique is chosen and assumed that the switches are ideal and their switching losses are zero. At the same time, inductor (P.L.) and capacitor (Q.C.) drops are insignificant. By selecting the appropriate value of the capacitor, the voltage across the load can be maintained. In Fig.2, the Power supplied by V_1 source to the load for the time t_1 sec. While two sources are connected in series for t_2 sec. in last, both the sources are out of service for the time of t_4 sec.

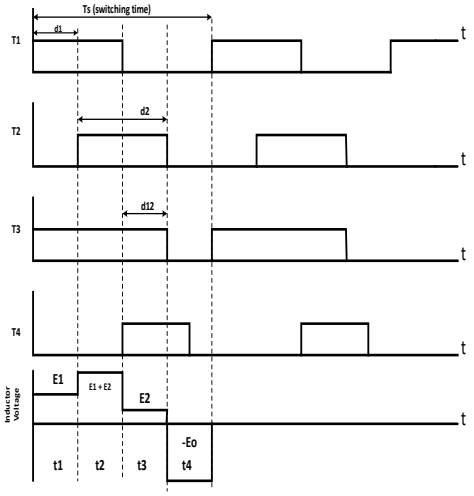


Fig. 1: Analysis of Inductor voltage waveforms

Therefore the value of inductor voltage can be calculated when switch T_1 is conducting for time duration t_1

$$e_L = e_1 * t_1 \quad (5)$$

During the time t_2, the voltage of Inductor is, existing.

$$e_L = (E_1 + E_2) * T_2 \quad (6)$$

The value of voltage across an inductor, when t_2 is on for a duration of time t_3 is

$$e_L = e_2 * t_3 \quad (7)$$

And, the value of e_L As soon as all switches of the converter are OFF for a time duration of T=t_4

$$e_L = (-E_0)T_{off} \quad (8)$$

According to the volt-second balance, the inductor voltage's average value should be zero in a steady-state condition. Therefore,

$$Average\ inductor\ voltage = \int_0^{Ts} e_L = 0 \quad (9)$$

Here,e_L = Inductor Voltage

$T_{S.}$ = switching time

$$T_S = \left(T_{on} + T_{off}\right) \quad (10)$$

Therefore,

$$\int_0^{Ts} e_L = (E_1 * t_1) + \left((E_1 + E_2) * t_2\right) + (E_2 + t_3) + (-E_0)T_{off} = 0 \quad (11)$$

The relationship between the input and output voltage equation can be obtained by solving the equation (11).

$$E_0 = \frac{E_1 d_1 + E_2 d_2}{(1 - d_1 - d_2 + d_{12})} \quad (12)$$

Where,

$$d_1 = \frac{t_1 + t_2}{t_s},\ d_2 = \frac{t_2 + t_3}{t_s} \text{ and } d_{12} = \frac{t_2}{T_s}$$

The value of capacitance and inductance, which will be used as filters, can be obtained from ripple voltage (Δv) of a capacitor and ripple current (Δi) of the Inductor, respectively.

$$\Delta i = \frac{E_0(1 - d_1 - d_2 + d_{12})}{L * f_s} \quad (13)$$

$$\Delta \mathrm{v} = \frac{E_0(d_1 + d_2 - d_{12})}{R * C * f_s} \quad (14)$$

3. A System Model And Design Of FPGA Based PID Regulator

The power stage of the converter:

The two different energy sources are being fed to the dual input DC-DC buck-boost converter, which regulates the output voltage.

The working of the controller:

The PID controller senses the error signal and generates the control signals, and then the modulator converts control signals into PWM signal to regulate the output voltage.

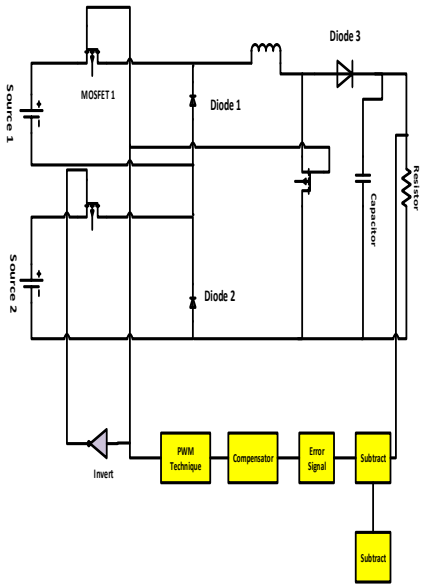


Fig. 2: System Model of closed-loop control of Dual input DC-DC buck-boost converter.

3.1. Implementation of PID Controller in FPGA

The type of linear controller is the PID controller is straightforward and has easy mathematical modeling by comparing it with the controller of the non-linear type. PID consists of a Proportional (P), Integral (I), and Derivative (D) controller. PID controller provides particular control action to the process by tuning these three parameters of proportional, Integral, and derivative of the PID controller. There are several tuning methods of the PID controller. There are multiple tuning methods for tuning the proportional, integral, and derivative values. One of them is the trial and error method that will be used in this paper [14].

3.1.1. Hardware Co-Simulation

Before implementing the PID algorithm onto the ASIC, We need to verify the working functionality that is all about hardware co-simulation [14]. The XSG is the platform that receives input vectors from the MatLab simulation and sends it to the FPGA kit. On the other hand, it receives output vectors from FPGA and sends them to MATLAB to perform its work and display the desired results.

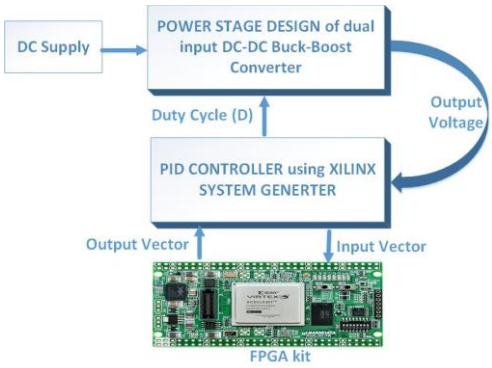


Fig. 3: Block diagram of Hardware co-simulation

The power stage of the dual input DC-DC converter has given feedback, which includes reference quantity, controller, and PWM strategy. The controller used is FPGA-based PID, which generates a control signal which can be further converted into a PWM signal and will be sent to the switches to perform its function. The working of the whole system is shown in fig. 3. Implementation of the PID controller on FPGA is done by using the XSG in MATLAB and Xilinx ISE design suite platforms, which is explained in Fig.04.

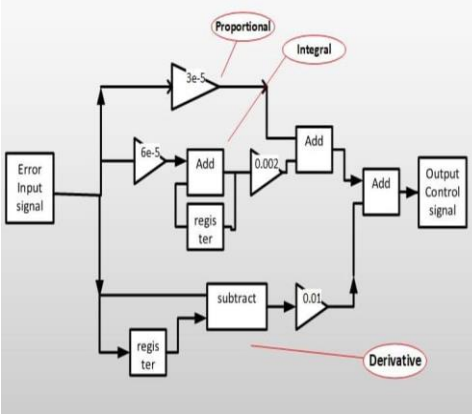


Fig. 4: Design of PID Controller using Xilinx System Generator

4. Results and Discussion

The two sources are given as an input to the dual input DC-DC converter. The values for the two sources are 10V and 5V. The power stage design of this converter was explained previously. The closed-loop control is designed and simulated, followed by the PID controller as a compensator.

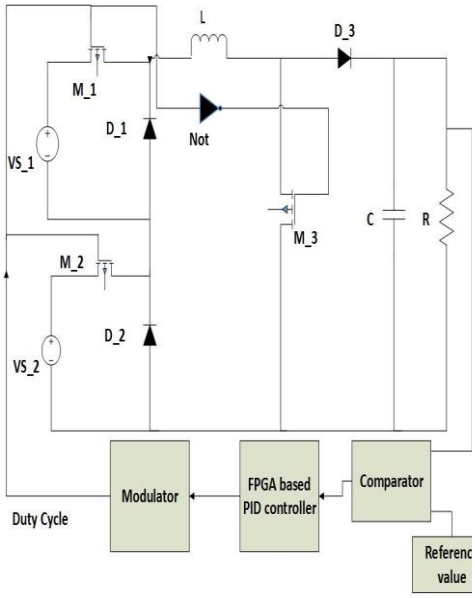


Figure No.05 Circuit Diagram of Dual input DC-DC Converter

The above circuits represent dual input DC-DC buck-boost converter, which maintains the required D.C. output voltage. The above circuit represents dual input DC-DC converter feed by two sources of energy. The converter's control is being done using PID controller, which is designed by using XSG and then generating a VHDL code to download into FPGAs Vitex5 and Virtex7 to observe the performance of these FPGA kits and also verify the results using hardware co-simulation. The virtex family used in this paper is because this family has high performance and capability as compared to the Spartan family FPGAs.

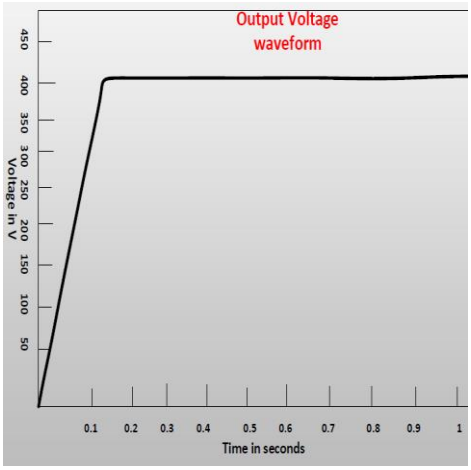


Fig. 6: Output Voltage of dual input DC-DC converter across the load

After designing the power stage and control of the dual input converter, the required output DC-DC voltage is verified using Hardware Co-simulation, which is, in this case, is D.C. 400V.

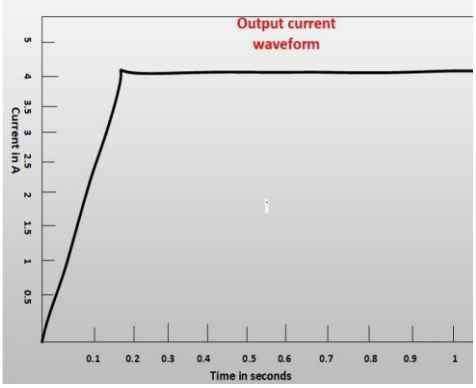


Fig. 7: Output Current of dual input DC-DC converter across the load

The PID controller's tuning is done based on the trial and error method to set the parameters of Proportional, Integral, and derivative. The PID controller's accurate tuning results in the converter's exact output voltage and current across the load.

4.1. FPGA Resource utilization

The Virtex5 and Virtex7 are used for the given topology of the system. The utilization of resources for Virex5 and Virtex7 are listed below.

Table.1. comparison of FPGAs resource utilization

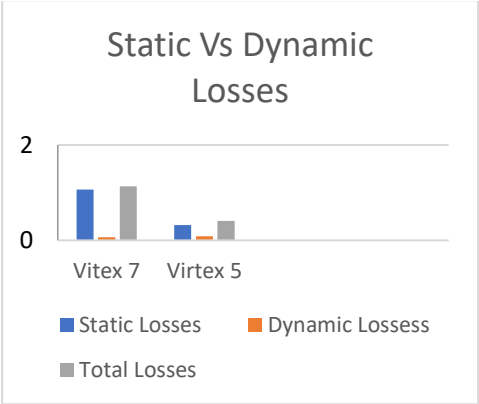
Resources	Virtex5			Virtex7		
	XC.5VLX50T-FF1136-1			XC7VX330T-2FFG1157		
	Used	Avail-able	Utili-ze	Used	Availa-ble	utilize
Number of Slice Registers	97	12480	1%	95	408000	1%
No. of Slice LUTs	3318	12480	26%	3405	204000	1%
No. of occupied Slices	1048	3120	33%	1008	51000	1%

As from the above table, the virtex5 has the least number of slice registers, lookup tables, and several occupied slices compared to virtex7.

4.1.1. Power Losses in Virtex7 and Virtex5

The virtex7 and virtex5 have many slice registers, LUTs, and occupied slices, so they are more efficient than previous FPGA kits.

Chart 1: Comparison of power losses in Virtex5 and Vitex7 kit



Total Power is 1.133W, the Power consumed by the dynamic and static types are 0.067W and 1.066W, respectively. Total Power is 1.133W, the Power consumed by the dynamic and static types are 0.084W and 0.405W, respectively.

The chart for the power consumption of FPGA is shown in chart 1.

5. Conclusion

The hardware co-simulation methodology is used to test the hardware performance—the whole system's simulation and the PID controller implements in Vitex5 and Virtex7 FPGA kits. The Virtex7 has maximum losses as compared to the virtex5. The converter's complex dynamic response is successfully received by a FPGA based PID controller. Results also validate that the negligible losses and no delay time is also achieved in proposed FPGA based PID controller, hence it is beneficial and efficient to implement a PID controller on FPGA quickly.

This work can be further implemented to cope up with the demands hybrid electric vehicles (HEV) with efficient dual input

converter provision. Moreover, The proposed converter topology has the advantage of regulating the voltage. So, this topology is also suitable for different voltage source as an input source.

AUTHOR CONTRIBUTION

All authors contributed equally to the work.

DATA AVAILABILITY STATEMENT

Not applicable

CONFLICT OF INTEREST

The authors declare no conflict of interest.

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