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MODELING OF HOT-CARRIER DEGRADATION BASED ON THOROUGH CARRIER TRANSPORT TREATMENT

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Abstract: We present and validate a physics-based model for hot-carrier degradation. The model is based on a thorough carrier transport treatment by means of an exact solution of the Boltzmann transport equation. Such important ingredients relevant for hot-carrier degradation as the competing mechanisms of bond dissociation, electron-electron scattering, the activation energy reduction due to the interaction of the dipole moment of the bond with the electric field as well as statistical fluctuations of this energy are incorporated in our approach. The model is validated in order to represent the linear drain current change in three different devices subjected to hot-carrier stress under different conditions. The main demand is that the model has to use a unique set of parameters. We analyze the importance of all the model ingredients, especially the role of electron-electron scattering. We check the idea that the channel/gate length of the device alone is not enough to judge whether electron-electron scattering is important or not and instead a combination of the device topology and stress conditions needs to be used.

Keywords: Hot-carrier degradation, interface traps, modeling, deterministic Boltzmann transport equation solver, MOSFET

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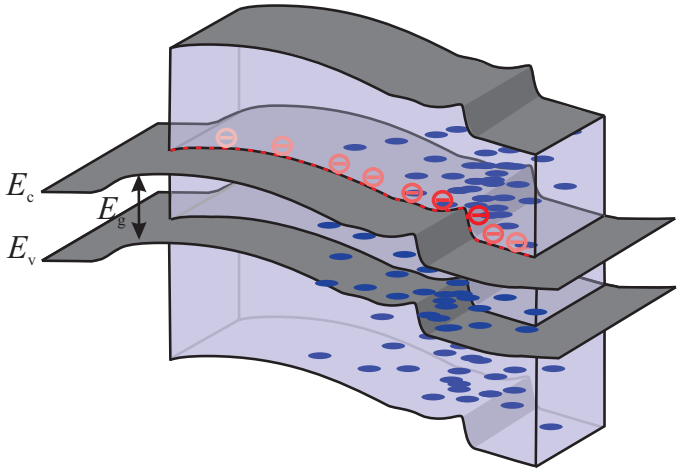

Fig. 1. A schematic representation of the MOSFET subjected to hot-carrier stress. The average carrier energy changes with the coordinate along the Si/SiO_2 interface, i.e. the carriers become hotter closer to the transistor drain. As a result, the bond-breakage rate and the interface state density are highest in this device area. The interface traps can capture charge carriers and become charged. They perturb the electrostatics of the device and scatter carriers, thereby degrading the device performance.

1 Introduction

Hot-carrier degradation (HCD) is a detrimental effect which degrades the metal-oxide-semiconductor field-effect transistor (MOSFET) performance and perturbs its characteristics. The damage is via generation of traps at or near the dielectric/Si interface of the MOSFET, see Fig. 1. These generated interface traps can capture electrons or holes and thus become charged. Therefore, the effect of charged defects on the device performance is twofold: they distort the local band-bending of the MOSFET and degrade the carrier mobility due to the additional scattering events at charges incorporated into the device. The former contribution results in the threshold voltage shift while the common action of both can be visible in degradation of the drain current, transconductance, on-state resistance, etc.

The HCD phenomenon was first reported in the 1970s [1–3] when transistor operating voltages were high. As a consequence, the high energetical fraction of the carrier ensemble was sufficiently populated. In other words, these *hot carriers* were able to efficiently trigger the bond dissociation events in a single collision with a Si-H bond, and thus this degradation mode was called "hot-carrier degradation". However, the aggressive scaling of MOSFETs has resulted, among other things, in substantially reduced operating/stress volt-

ages. Under these conditions, the hot carriers have negligible concentrations and the single-particle bond-breakage process thus has a rather low rate. Instead, several *colder carriers* can induce a multiple vibrational excitation (MVE) of the bond which triggers a bond rupture event [4–10]. Therefore, one can say that there are two competing HCD modes: single- and multiple-particle processes (SP- and MP-processes) which are triggered by hot and cold carriers.

As for the driving force of hot-carrier degradation, its understanding has also been changed. One of the pioneering HCD concepts [3, 11] – the so-called lucky electron model – states that an electron which has gained sufficiently high energy without loosing energy and scattering back into the channel can overcome the potential barrier at the Si/SiO_2 interface, penetrate the SiO_2 conduction band, and generate defect(s). Since this lucky electron obtains energy from the electric field, HCD was suggested to be field-driven. This understanding, however, needed to be reconsidered after a series of experiments published by the IBM group [12, 13]. The authors performed different types of stress (channel and substrate hot electron/hole stresses as well as Fowler-Nordheim and direct tunneling injections) and showed that in all cases the interface state generation rate depends only on the energy deposited by carriers and is insensitive to the electric field. This idea was implemented within the so-called energy driven paradigm proposed by Rauch and La Rosa [8, 14, 15].

The information on what exact portion of energy is deposited by carriers can only be obtained from a thorough carrier transport treatment. This task, however, is computationally very demanding– and this is the reason why a lot of hot-carrier degradation models are empirical or at best phenomenological [3, 16–22]. Furthermore, some simplifications are often made also in physics-based models of hot-carrier degradation. For instance, the SP- ans MP-mechanisms are competing pathways of the same bond dissociation reaction and need to be considered self-consistently. However, for the sake of simplicity in some HCD models these processes are treated as being independent [23–27]. The rates of these processes are affected by the scattering mechanisms with corresponding rates determined by the MOSFET configuration and applied voltages. In scaled devices electron-electron scattering (EES) plays a significant role and impacts the kinetics of defect generation [28, 29]. However, in early versions of one of the most successful HCD models developed by the Bravaix group, three HCD modes, namely driven by the SP-process, by EES, and by the MP-mechanisms are distinguished and considered independently [23, 24, 30].

Another controversial issue is the role of electron-electron scattering in the context of HCD. On the one hand, Rauch and La Rosa have shown that EES is responsible for a severe hot-carrier damage enhancement in devices with channel lengths shorter than 80-100 nm [8, 28, 29]. This scattering mechanism also defines the temperature behavior in ultra-scaled devices [8]. On the other hand, the Bravaix group has recently suggested that in their transistors the role of EES is dramatically overestimated. Instead, in short-channel MOSFETs HCD has been suggested to be driven by the two particle mixed mode process [31].

In this work we present a physics-based HCD model which relies on a thorough carrier transport treatment. This treatment is based on an exact solution of the Boltzmann transport equation. The model captures such ingredients relevant for hot-carrier degradation as competing mechanisms of Si-H bond-dissociation, electron-electron scattering, the bond-breakage activation energy reduction due to the interaction of the electric field with the dipole moment of the bond and statistical variations of this energy. To validate the model we use HCD data obtained in nanoscale transistors. We also analyze the role of each particular model component.

2 Characteristic features of hot-carrier degradation

A principal question which needs to be addressed first of all is: "what is the criterion which allows us to separate hot and cold carriers?". Under "hot carriers" we understand those carriers with energies above the activation energy for the Si-H bond dissociation reaction, i.e. particles with energies above $\sim$1.5 eV [6, 32]. In fact, the interface between a crystalline Si substrate and an amorphous SiO_2 layed is imperfect. The disorder at the interface leads to Si- dangling bonds, see Fig. 2. These bonds can capture charge carriers. This process converts them to electrically active defects. To prevent this, hydrogen is intentionally incorporated into devices at the post-oxidation step. When H atoms terminate the Si- bonds, neutral and electrically passive Si-H bonds are formed, Fig. 2. The reverse process of bond depassivation can be triggered if a bond-breakage portion of energy is transferred to these Si-H bonds by e.g. hot carriers. The activation energy E_a for this process was shown to be $\sim$1.5 eV [6, 32].

A solitary high energetical carrier can induce a bond-breakage event in a single collisions, i.e. can trigger the SP-process, see Fig. 3. Due to the huge disparity between the electron mass and the mass of the hydrogen nucleus and the total momentum conservation only a negligibly small portion of en-

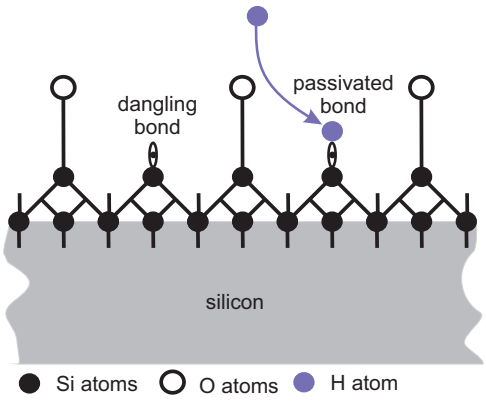

Fig. 2. A dangling Si- bond is electrically active. i.e. can capture electrons/holes, become charged distort the MOSFET characteristics. To prevent this, hydrogen is intentionally introduced into the device. H atoms terminate dangling bonds and form electrically passive Si-H bonds.

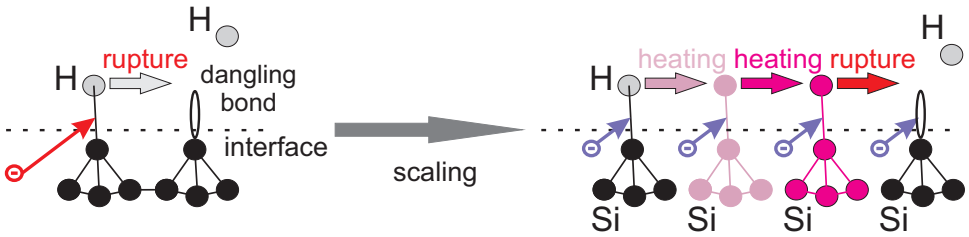

Fig. 3. Bond dissociation by a solitary high energetical carrier and by a series of colder carriers. The former scenario is typical in long-channel MOSFETs subjected to hot-carrier stress at high voltages, while the latter one corresponds to short-channel devices stressed at low voltages.

ergy will be transferred to H, which is not sufficient for hydrogen release. Instead, most likely, the hot electron impinging on the bond can excite one of the bonding electrons to an antibonding (AB) state [33, 34]. Therefore, we further label this process as AB-mechanism. Since the activation energy for bond-breakage is ∼1.5 eV hot-carrier degradation was expected to be almost completely suppressed if the applied source-drain V_{ds} voltage is below 1.5 V. In practice, however, these expectations were debunked and HCD was shown to be quite severe even at low V_{ds} [35]. There are two reasons responsible for substantial HCD in scaled devices: the multiple-carrier mechanism for bond dissociation and energy exchange mechanisms which populate the high energy fraction of the carrier ensemble. The multiple-carrier mechanism is related to the bombardment of the bond by a series of colder carriers which induce the multiple vibrational excitation (MVE) of the bond followed by

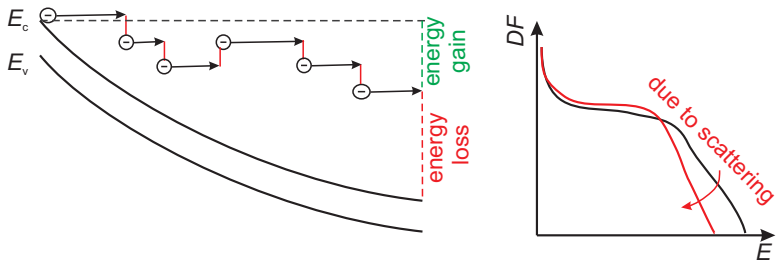

Fig. 4. A schematic representation of scattering mechanisms leading to energy loss. These mechanism depopulate the high energetical fraction of the carrier ensemble. In other words, they suppress the high-energy tails of the carrier energy distribution function.

hydrogen release, and hence by bond dissociation [6]. The MVE theory was first applied to interpret experimental data on hydrogen/deuterium desorption from H/D-passivated Si surfaces induced by electrons tunneling from a scanning tunneling microscope tip [36–38]. This theory was then adopted by the group of Hess for the case of Si/SiO_2 interfaces subjected to hot-carrier stress under conditions with low average carrier energies [33, 39, 40].

At the device level, the interaction between these single- and multiple-carrier pathways of bond dissociation leads to the change of the worst-case conditions (WCC) of HCD. Thus, in long-channel devices HCD is most severe when the average carrier energy has a maximum. In the case of n-MOSFETs the criterion chosen to judge on HCD severity is the substrate current [41–43]. This current consists of majority carriers generated by impact ionization. Both SP-process and impact ionization are characterized by rates of a same functional structure [29], and therefore the impact ionization induced substrate current is used to judge about the SP-process (i.e. HCD) intensity. As for p-MOSFETs, due to similar reasons the gate current is used as an indicator of the HCD severity [43–45]. In the former case the worst-case conditions are obtained when $V_{gs} \sim (0.4\text{-}0.5)V_{ds}$ (V_{gs} is the gate voltage) while for the latter case such an empirical interrelation between the voltages is not established. As for the case of scaled transistors, rather than the average particle energy the carrier flux is important. This is the case when $V_{gs} = V_{ds}$ for both n- and p-MOSFETs [46–49].

As for the scattering mechanisms, they can populate the fraction of the carrier packet up to energies which are much higher than those available from the contact bias. Most important among them are impact ionization [50], Auger recombination [51], electron-phonon [52], and electron-electron scattering [53, 54]. Among these mechanisms electron-electron scattering is of special importance in ultra-scaled devices. EES also changes the temper-

ature behavior of HCD. In fact, in long-channel devices HCD becomes less pronounced at elevated temperatures [22, 41, 55–58]. The reason is that the scattering mechanisms depopulate the high energetical fraction of the carrier ensemble. Mathematically this means that high-energy tails of the carrier energy distribution function (DF) (which represents the probability to find carriers in the elementary energy range of $[E; E + \mathrm{d}E]$) are suppressed due to these mechanisms, see Fig. 4. The rates of these processes increase with temperature, thereby making suppression of hot carriers more efficient at higher temperatures and, as a result, weaken hot-carrier degradation. In ultra-scaled devices, however, such events as electron-phonon scattering and scattering at ionized impurities are not efficient because a channel electron "meets" just a few dopant/lattice atoms. Vice versa, the carrier concentrations are high in these devices and the EES process can be quite efficient. EES was shown to populate the high-energy tails and therefore enforce hot-carrier degradation. Since the electron-electron interaction rate increases with temperature, EES leads to more severe HCD in scaled transistors. This trend is confirmed by the experimental data [59–61].

Since hot-carrier degradation is an energy driven process, carriers need to travel some distance to gain sufficient energy from the electric field. Such a behavior is typical also for the case of cold carriers because the rate of the MP-process depends on the carrier flux, i.e. also on the carrier velocity/energy. This determines one of the main features of hot-carrier degradation: the strong localization of the damage [62–64]. Let us consider an n-channel MOSFET with the electron packet moving from the source to the drain. It is well known that the maximum electric field, carrier temperature and the average carrier energy peak near the drain end of the gate. As a result, in the lucky electron model as well as in the energy driven paradigm the bond-breakage rate, and hence the interface state density N_{it}, have their maxima also in this region, see Fig. 5. From Fig. 5,right one can also see that the maximum of the interface state density coincides neither with the electric field peak nor with the maximum of the carrier temperature/energy. Instead, we have recently shown [27, 65, 66] that the quantity which controls hot-carrier degradation is the carrier acceleration integral (AI) which will be introduced below.

All the peculiarities of hot-carrier degradation suggest that the bond-breakage kinetics are determined by the distribution of the carriers over the energy, that is, by the DF. Therefore, a proper description and modeling of HCD need to be based on a thorough carrier transport treatment.

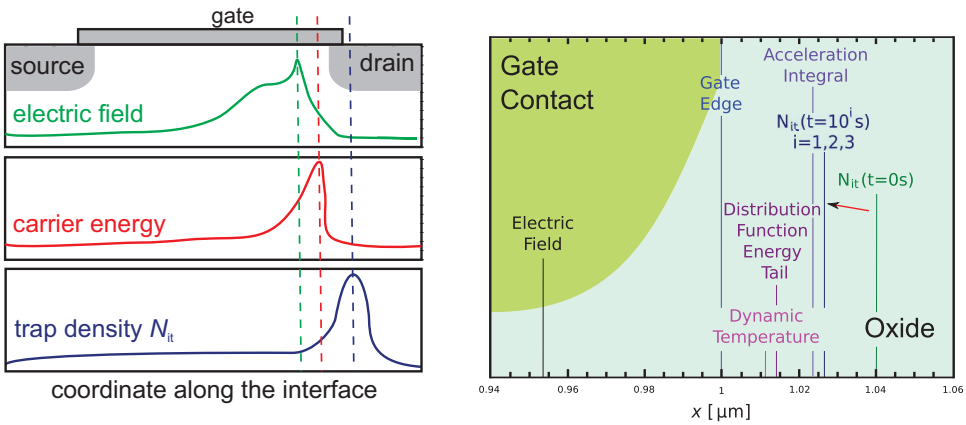

Fig. 5. **Left**: Schematic representation of electric field, average carrier energy and interface state density profiles. **Right**: Positions of maxima of quantities crucial for HCD: electric field, carrier dynamic temperature, carrier average energy, interface trap density, etc. These exemplary simulations were preformed for a 5V n-MOSFET fabricated on a standard 0.35 μm process with a gate length of 0.5 μm subjected to hot-carrier stress at $V_{\mathrm{ds}} = 6.25\,\mathrm{V}$ and $V_{\mathrm{gs}} = 2.0\,\mathrm{V}$.

3 The model

Our physics-based HCD model aims at covering and linking all the levels related to the hot-carrier degradation phenomenon starting at the microscopic level of defect generation which is connected via the carrier transport treatment with the modeling of the degraded devices. Thus, the model includes three corresponding modules, see Fig. 6. The transport kernel is realized on the platform of the deterministic Boltzmann transport equation solver ViennaSHE [67–69]. ViennaSHE incorporates full-band effects as well as such energy exchange mechanisms as scattering at ionized impurities, surface scattering, electron-electron and electron-phonon interactions as well as impact ionization. ViennaSHE is used to evaluate the carrier energy distribution functions for a particular device topology and given stress/operating conditions.

The obtained carrier DFs are then used to calculate the carrier acceleration integral which determines the rates of both AB- and MVE-mechanisms. This acceleration integral for electrons/holes and AB/MVE-processes is defined as:

$$I_{\mathrm{ab/mve}}^{(\mathrm{e/h})} = \int_{E_{\mathrm{th}}}^{\infty} f^{(\mathrm{e/h})}(E) g^{(\mathrm{e/h})}(E) \sigma_{\mathrm{ab/mve}}^{(\mathrm{e/h})}(E) v(E) dE, \tag{1}$$

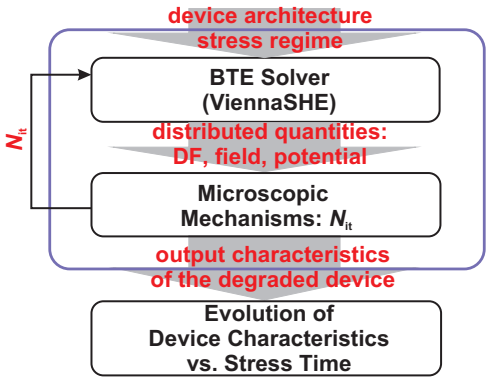

Fig. 6. Our physics-based HCD model contains three main modules: a description of the defect generation kinetics, the carrier transport kernel, and modeling of the degraded devices. The model is implemented into the deterministic solver of the Boltzmann transport equation ViennaSHE.

where $f^{(\mathrm{e/h})}(E)$ stands for the DFs, $g^{(\mathrm{e/h})}(E)$ the corresponding density-of-states, $\sigma_{\mathrm{ab/mve}}(E)$ the reaction cross section, while $v(E)$ the group velocity. To model the reaction cross section in the case of the AB-process we use a Keldysh-like expression [4, 50]:

$$\sigma^{(\mathrm{e/h})}_{\mathrm{ab/mve}}(E) = \sigma^{(\mathrm{e/h})}_{0,\mathrm{ab/mve}}(E - E_{\mathrm{th,ab/mve}})^{p_{\mathrm{it}}}. \tag{2}$$

Here $\sigma_{0,\mathrm{ab/mve}}$ is a prefactor, $E_{\mathrm{th,ab/mve}}$ is the bond-breakage energy, while $p_{\mathrm{it}} = 11$. Note that the activation energy can vary statistically because of the structural disorder at the Si/SiO_2 interface and due to the interaction of the electric field with the dipole moment of the bond. As for the MVE-mechanism we consider the Si-H bond as a truncated harmonic oscillator characterized by a system of eigenstates in the corresponding potential profile well, see Fig. 7. Thus, in the case of the MVE-process the threshold energy is the distance between the oscillator levels $\hbar\omega$. It is important to emphasize that in the previous version of our HCD model we considered the single- and multiple-carrier mechanism as independent processes and the cumulative interface state density N_{it} was calculated as the sum of SP- and MP-induced contributions weighted with some probability factors (fitting parameters of the model), cf. [26, 27], Fig. 7,left. In the current version of our model we incorporate all the superpositions of the AB- and MVE-mechanisms [70, 71], see Fig. 7,right. In other words, first the bond can be heated by several colder particles (which trigger the MVE-mechanism) to an intermediate level with the index i and then dissociated by a single carrier with relatively high energy. If the bond is in the ith eigenstate the potential barrier for the

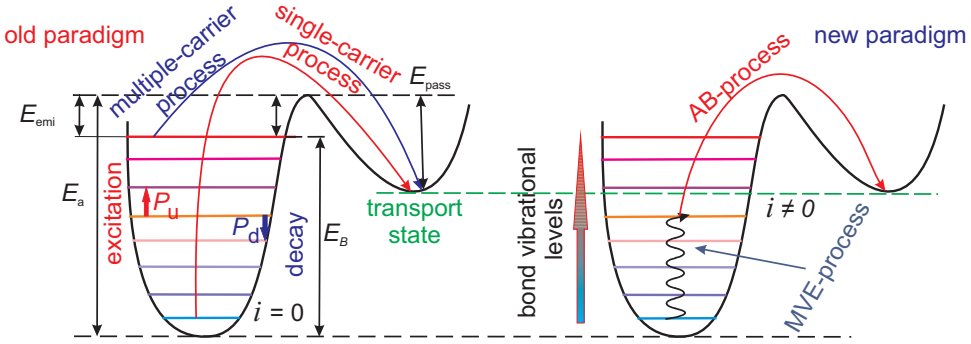

Fig. 7. The Si-H bond as truncated harmonic oscillator. **Left**: In the previous version of our HCD model the single- and multiple-carrier processes are modeled as independent processes. **Right**: In the most recent version of our model these processes are considered as competing pathways of the same bond-breakage reaction. We take into account all the possible superpositions of the AB- and MVE-mechanisms when first the bond is pre-heated by a series of low energetical carriers (the MVE-mode) and then ruptured by a solitary hot carrier (AB-mechanism).

proton which separates this state and the transport mode is reduced, and thus the acceleration integral is:

$$I_{\mathrm{ab},i} = \int f(E)g(E)\sigma_0(E - E_\mathrm{a} + E_i + d \times E_\mathrm{ox})^{p_\mathrm{it}} v(E)\mathrm{d}E. \tag{3}$$

Here E_i is the level position and the term $d \times E_\mathrm{ox}$ represents the activation energy reduction caused by the interaction of the dipole moment of the bond d with the oxide electric field E_ox. As a result, bond dissociation from the intermediate level i requires a lower carrier energy and the probability that the ensemble contains particles with energies above this threshold is higher. The bond-breakage rate from each particular level is modeled as

$$R_{\mathrm{ab},i} = w_\mathrm{th} \exp\left[-\left(E_\mathrm{a} - E_i - d \times E_\mathrm{ox}\right)/k_\mathrm{B}T\right] + I_{\mathrm{AB},i}. \tag{4}$$

where the first term (with the attempt frequency w_th) corresponds to the thermal activation of the H atom over the potential barrier, while the acceleration integral $I_{\mathrm{AB},i}$ represents the effect of hot carriers.

The bond dissociation kinetics are described by the set of rate equations:

$$\begin{aligned}
\frac{\mathrm{d}n_0}{\mathrm{d}t} &= P_\mathrm{d} n_1 - P_\mathrm{u} n_0 - R_{\mathrm{a},0} n_0 + R_{\mathrm{p},0} N_\mathrm{it}^2 \\
\frac{\mathrm{d}n_i}{\mathrm{d}t} &= P_\mathrm{d}(n_{i+1} - n_i) - P_\mathrm{u}(n_i - n_{i-1}) - R_{\mathrm{a},i} n_i + R_{\mathrm{p},i} N_\mathrm{it}^2 \\
\frac{\mathrm{d}n_{N_l}}{\mathrm{d}t} &= P_\mathrm{u} n_{N_l - 1} - P_\mathrm{d} n_{N_l} - R_{\mathrm{a},N_l} n_{N_l} + R_{\mathrm{p},N_l} N_\mathrm{it}^2.
\end{aligned} \tag{5}$$

Note that in contrast to the system used in the Bravaix model we also consider passivation reactions to each particular level i with the corresponding rates $R_{\mathrm{p},i}$. In (5) n_i are the level occupation numbers, N_l labels the last bonded state and P_u and P_d are the rates of the multivibrational mode excitation/deexcitation processes:

$$\begin{aligned} P_\mathrm{u} &= \omega_\mathrm{e}\exp\left(-\hbar\omega/k_\mathrm{B}T_\mathrm{L}\right) + I_\mathrm{MVE}, \\ P_\mathrm{d} &= \omega_\mathrm{e} + I_\mathrm{MVE} \end{aligned} \tag{6}$$

with ω_e being the reciprocal phonon life-time.

We solve the system (5) by taking into account the huge disparity between the characteristic times which describe the establishment of the oscillator steady-state and those which correspond to the bond rapture/passivation processes.

$$\frac{\mathrm{d}N_\mathrm{it}}{\mathrm{d}t} = \left(N_0 - N_\mathrm{it}\right) R_\mathrm{a} - N_\mathrm{it}^2 R_\mathrm{p}, \tag{7}$$

where N_0 is the concentration of passivated Si-H bonds and the cumulative bond-breakage rate is:

$$R_\mathrm{a} = \frac{1}{k}\sum_i R_{\mathrm{a},i}\left(\frac{P_\mathrm{u}}{P_\mathrm{d}}\right)^i, \tag{8}$$

where k is is a normalization prefactor:

$$k = \sum_i \left(\frac{P_\mathrm{u}}{P_\mathrm{d}}\right)^i. \tag{9}$$

As for the cumulative passivation rate $R_\mathrm{p} = \sum_i P_i$, without loss of generality, one may represent the P rate by the Arrhenius term for thermal activation over a single barrier, i.e.

$$R_\mathrm{p} = \nu_\mathrm{p}\exp(-E_\mathrm{pass}/k_\mathrm{B}T_\mathrm{L}), \tag{10}$$

where ν_p is a prefactor which designates the attempt frequency.

The system (5) is finally solved analytically:

$$\begin{aligned} N_\mathrm{it}(t) &= \frac{\sqrt{R_\mathrm{a}^2/4 + N_0 R_\mathrm{a} R_\mathrm{p}}}{R_\mathrm{p}}\frac{1 - f(t)}{1 + f(t)} - \frac{R_\mathrm{a}}{2R_\mathrm{p}}, \\ f(t) &= \frac{\sqrt{R_\mathrm{a}^2/4 + N_0 R_\mathrm{a} R_\mathrm{p}} - R_\mathrm{a}/2}{\sqrt{R_\mathrm{a}^2/4 + N_0 R_\mathrm{a} R_\mathrm{p}} + R_\mathrm{a}/2}\exp\left(-2t\sqrt{R_\mathrm{a}^2/4 + N_0 R_\mathrm{a} R_\mathrm{p}}\right). \end{aligned} \tag{11}$$

It is important to emphasize that this solution transforms to the expression obtained within the previous version of our HCD model when the AB- and MVE-mechanisms were considered independently, i.e. if the rate of one of the processes is neglected, cf. [26, 27].

The activation energy reduction due to the interaction between the oxide electric field and the dipole moment of the Si-H bond is modeled as $d \times E_{\mathrm{ox}}$, cf. (3), see [72, 73]. The dipole moment of the bond is a fitting parameter of the model. In the case of the SiON gate films of n-MOSFETs employed to validate the model we use a value of $d = 0.044$ which is slightly different from that used in the Bravaix model (0.056) [73]. As for the activation energy fluctuations we assume that E_{a} obeys a Gaussian distribution with the mean values and standard deviation of $\langle E_{\mathrm{a}} \rangle = 1.5\,\mathrm{eV}$ and $\sigma_{\mathrm{E}} = 0.15\,\mathrm{eV}$. These values are in good agreement with experimentally observed ones [74–76]. The effect of the activation energy dispersion was incorporated in the manner that the range $[\langle E_{\mathrm{a}} \rangle - 3\sigma_{\mathrm{E}}; \langle E_{\mathrm{a}} \rangle + 3\sigma_{\mathrm{E}}]$ was discretized and for each discretization point we evaluated the interface trap density profile $N_{\mathrm{it}}(x)$ according to (11) weighted with the Gaussian distribution.

4 Results and Discussion

The model was validated in a manner to capture HCD in different devices stressed under various hot-carrier conditions but using a unique set of the model parameters. The aim was also to analyze the importance of each of the model ingredients, especially the role of the EES process in the context of hot-carrier degradation.

4.1 Experiment

To validate the model we used SiON n-MOSFETs of an identical architecture but with different gate lengths, i.e. $L_{\mathrm{G}} = 65$, 100, and 150 nm, which corresponds to the channel lengths of ~ 45, 80, and 120 nm. A 2.5 nm thick SiON gate film was fabricated by a decoupled plasma nitridation process followed by post-nitridation annealing. The devices were subjected to hot-carrier stress at the worst-case HCD conditions corresponding to these particular MOSFETs and at two different drain voltages: $V_{\mathrm{ds}} = 1.8$ and 2.2 V for approximately 8 ks at room temperature. During stress the normalized linear drain current change, i.e. $|I_{\mathrm{dlin}}(t) - I_{\mathrm{dlin},0}|/I_{\mathrm{dlin},0}$, was recorded as a function of stress time (here $I_{\mathrm{dlin}}(t)$ is the linear drain current at stress time t, while $I_{\mathrm{dlin},0}$ is the drain current measured in the fresh device).

The MOSFET with $L_G = 65\,\text{nm}$ was treated as a short-channel device with corresponding worst-case scenario realized when $V_{gs} = V_{ds}$. As for the 150 nm counterpart it was not obvious whether this MOSFET belongs to the long-channel devices or not. To check this, the substrate current was recorded as a function of V_{ds} and V_{gs}. The substrate current maximum was observed at $V_{gs} \sim V_{ds}/2$. This finding suggests that this is a long-channel MOSFET with the corresponding worst-case combination of stress voltages. In the case of the 100 nm transistor the substrate current was at maximum when $V_{gs} = 2/3V_{ds}$ and this relation between V_{ds} and V_{gs} was used to stress this transistor.

4.2 The distribution functions

The device architecture was obtained using the Sentaurus Process simulator [77]. Since the carrier distribution functions are very sensitive to doping profiles, the process and device simulators (i.e. Sentaurus Process and ViennaSHE) were coupled and calibrated in a fashion to represent the current-voltage characteristics of the fresh device.

A series of electron DFs computed with ViennaSHE for 65 and 150 nm MOSFETs stressed at $V_{ds} = 2.2\,\text{V}$ are shown in Fig. 8. These DFs are calculated with and without EES and plotted in different positions in the device (in the graph the distance from the source to the position where the DF is evaluated is marked). The DFs are severely non-equilibrium, i.e. they show a plateau at moderate energies and prominent high-energy tails. These high-energy tails become more populated due to electron-electron scattering, and thus one concludes that the effect of EES substantially changes the shape of the distribution functions. These changes are especially strong near the drain but less pronounced near the source. One can also see that the onset of the characteristic hump visible in the high-energy tails (which is a result of EES) occurs at higher energies in the 150 nm device, and this suggests that the effect of EES is expected to be weaker in longer transistors. Note that all the DFs still have a Maxwellian rudiment at low energies. This rudiment becomes longer near the source, i.e. the distribution functions are closer to the equilibrium ones.

These distribution functions are used to evaluate the carrier acceleration integrals. The AIs evaluated for the ground state and for the case of the same devices and same stress conditions as Fig. 8 are plotted in Fig. 9. To check the effect of EES the AIs obtained without this scattering mechanism are also shown. One can see that EES substantially changes the AI shape. The

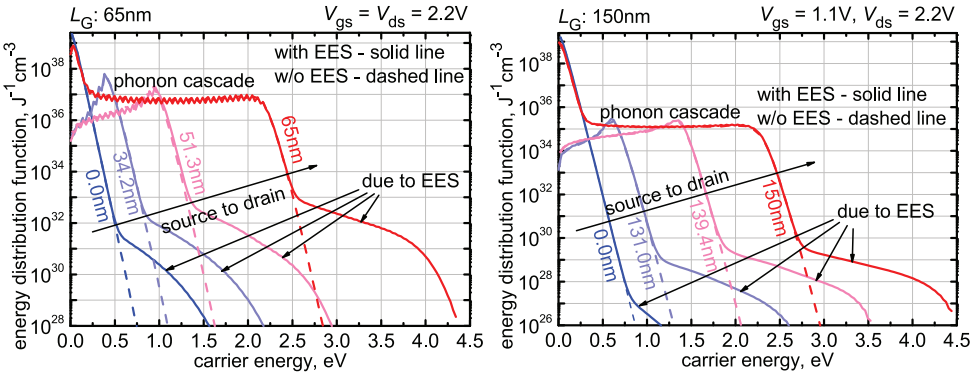

Fig. 8. A family of the carrier distribution functions calculated for the 65 and 150 nm MOSFETs stressed at the corresponding worst-case HCD conditions at $V_{\rm ds} = 2.2$ V with and without electron-electron scattering. The DFs are plotted in different positions of the transistors at the SiON/Si interface.

impact of EES on the AI is weaker in longer devices. This finding correlates with the DFs shown in Fig. 8 where the high-energy tails are more populated by electron-electron scattering in the shorter MOSFET.

4.3 The $\Delta I_{\rm dlin}$ data and $N_{\rm it}(x)$ profiles

Fig. 10 summarizes the experimental linear drain current change plotted vs. stress time for all the devices and all combinations of stress voltages as well as simulated $\Delta I_{\rm dlin}(t)$ curves. One can see that agreement between experiment and theory is rather good. It is also important to emphasize that the model uses a unique set of parameters for all devices/conditions. To

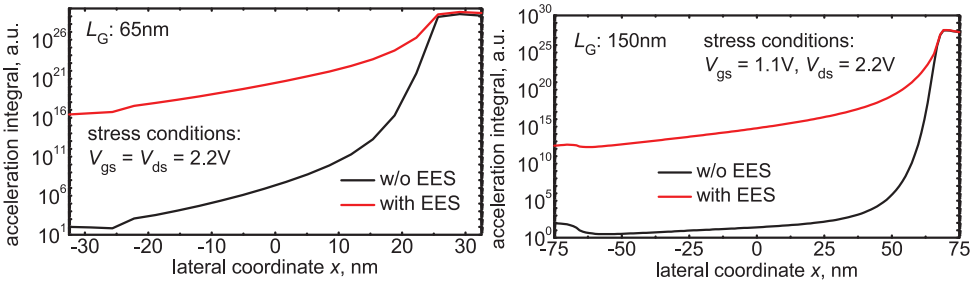

Fig. 9. The carrier acceleration integral plotted for the 65 and 150 nm devices stressed at $V_{\rm ds} = 2.2$ V vs. the lateral coordinate x along the dielectric/Si interface. These integrals are evaluated with and without electron-electron scattering. One can see that the effect of EES is strong. The source corresponds to x = -32.5 and -75 nm for 65 and 150 nm devices, respectively.

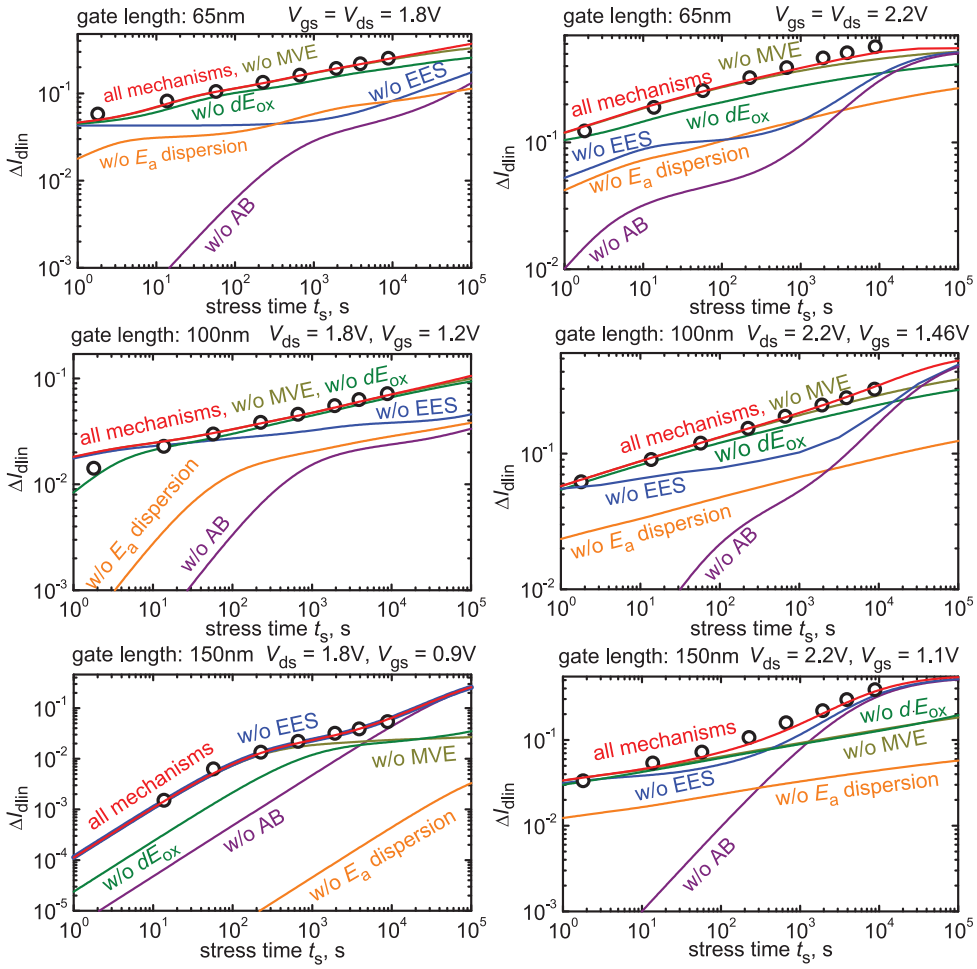

Fig. 10. The normalized change of the linear drain ($|I_{\mathrm{dlin}}(t) - I_{\mathrm{dlin},0}|/I_{\mathrm{dlin},0}$) current as a function of stress time: the experimental data vs. the simulated curves plotted for three n-MOSFETs with gate lengths of 65, 100, and 150 nm stressed at their HCD worst-case conditions and two different $V_{\mathrm{ds}} = 1.8$ and 2.2 V. One can see that agreement between experiment and simulations is good. To analyze the importance of particular model components we have also plotted $\Delta I_{\mathrm{dlin}}(t)$ curves obtained neglecting one of the model components such as AB- and MVE-mechanisms, EES, the $d \times E_{\mathrm{ox}}$ activation energy reduction, and its dispersion.

analyze the importance of each particular model component (competing AB- and MVE-processes, electron-electron scattering, interaction of the dielectric electric field with the dipole moment of the bond, and the activation energy dispersion) we have also simulated $\Delta I_{\mathrm{dlin}}(t)$ dependences disregarding one of these components.

One can see that even in the case of scaled devices with $L_{\mathrm{G}} = 65\,\mathrm{nm}$ the AB-process plays a dominant role, especially at short stress times but is less pronounced at longer stress times. This tendency can be understood if we consider the $N_{\mathrm{it}}(x)$ profiles. Fig. 11 depicts these profiles obtained for the 65 nm transistor stressed at $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$ for each stress time step with and without one of the model ingredients. One can see that the concentration N_{it} peaks near the drain, while near the source N_{it} is lower and the profile is almost flat. The drain peak corresponds to the effect of hot carriers. Indeed, near the drain carriers are characterized by most pronounced high-energy tails of the distribution functions, cf. Figs. 8, 9. Thus, if the AB-mechanism rate is suppressed the drain peak appears to be narrower and weaker. At the same time, the source acts as a reservoir of thermalized carriers with DFs revealing almost Maxwellian behavior. Note that already at a stress time of 1.8 s the drain peak is saturated, i.e. N_{it} does not change with either the lateral coordinate x nor with stress time. As a result, short-term HCD is determined by the propagation of the N_{it} front towards the device center, and hence, ignoring of the AB-process leads to a sever ΔI_{dlin} underestimation especially at short times.

It is important to emphasize that the contribution of the AB-mechanism is more pronounced in shorter devices. At a first glance this trend contradicts the commonly used idea that hot-carrier degradation is controlled by the AB-process in long-channel devices and the role of this mechanism becomes less pronounced if device dimensions shrink. To analyze this behavior in more detail we also have plotted the electron DFs for all three devices and the same combination of stress voltages ($V_{\mathrm{ds}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$), see Fig. 12. One can see that the DFs have lower values in the case of longer devices. Thus, the distribution function values calculated for the 65 and 150 nm device can differ by a factor of ~ 7 at moderate energies and this difference is even more pronounced at high-energy tails. As the AB-mechanism is very sensitive to the high-energy tails, its relative contribution is less important in the case of longer MOSFETs.

Ignoring electron-electron scattering leads to the same tendencies as suppressing the AB-process rate, see Fig. 10 and Fig. 11. For instance, one can see that the drain N_{it} maximum also becomes narrower, while ΔI_{dlin} appears to be underestimated especially at moderate stress times (at longer times the EES effect is weaker). This is because EES populates the high energy fraction of the carrier ensemble (see Fig. 8), and therefore strengthens the AB-mechanism. It is important to emphasize that the contribution of electron-electron scattering is less pronounced in longer devices. For exam-

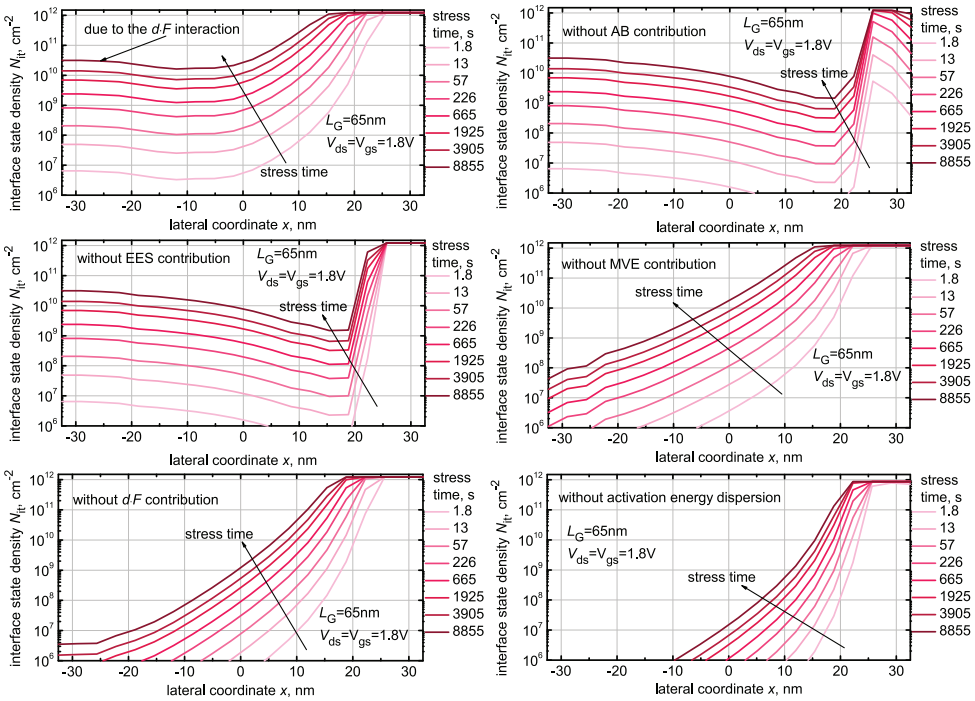

Fig. 11. The interface state density $N_{\mathrm{it}}(x)$ profiles plotted for the 65 nm transistor subjected to hot-carrier stress at $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8$ V for all stress time steps obtained with the "full" model and neglecting one of the model components. The source corresponds to $x =$ -32.5 nm.

ple, the EES effect is weak in the 100 nm transistor at $V_{\mathrm{ds}} = 1.8$ V and $V_{\mathrm{gs}} = 1.2$ V and can be neglected in the 150 nm counterpart at both combinations of V_{ds} and V_{gs}. This tendency can be explained from an analysis of electron DFs plotted with and without EES, see Fig. 8. One can see that at the same stress voltages the onset of the EES-related hump visible in high-energy tails occurs at higher energies, thereby leading to a weaker EES impact.

The interaction of the electric field with the dipole moment of the bond leads to a secondary maximum observed in the $N_{\mathrm{it}}(x)$ profiles near the drain Fig. 11. This situation is typical for all three devices stressed under different interrelations between V_{ds} and V_{gs}, see Fig. 13. This maximum coincides with the the maximum of the electric field which is also located near the source. To illustrate this, we have evaluated the electric field as a function of the lateral coordinate x along the interface for two devices (with gate lengths of 65 and 150 nm) for both combinations of stress voltages. One can see that in all four cases the electric field profiles reveal maxima near the source and the positions of these maxima coincide with the N_{it} peak positions, cf. Fig.

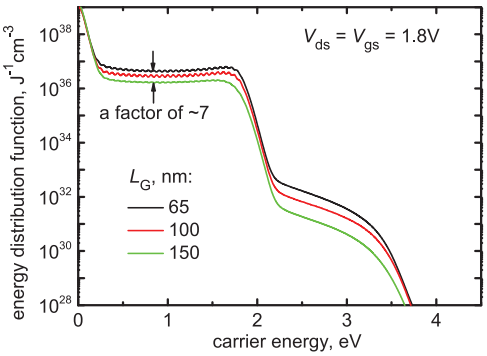

Fig. 12. The carrier energy distribution functions computed for $V_{\rm gs} = V_{\rm ds} = 1.8\,{\rm V}$ for all the devices for the drain area. One can see that at the same combination of applied voltages DFs are characterized by lower values.

13. If the $d \times E_{\rm ox}$ activation energy reduction is ignored, the interface states density profiles are flat in the source section of the device. These constant $N_{\rm it}(x)$ dependences are related to the saturated MVE-process. Note that quite a similar behavior of $N_{\rm it}$ curves was reported in our previous works also for the case of a long-channel n-MOSFET with the gate length of $0.5\,\mu$m [25–27] as well as independently by the Bravaix group [78]. The secondary $N_{\rm it}$ maximum is more pronounced at long stress times and thus determines the long-term linear drain current change, see Fig. 10 .

As for the MVE-process, Fig. 10 suggests that its role becomes more important in longer devices. At a first glance, this results appears to be quite unusual because the MVE-process is assumed to be dominant in short-channel devices. The reason is the same as the explanation why the AB-mechanism contribution is more pronounced in MOSFETs with longer $L_{\rm G}$. At a fixed pair of $V_{\rm ds}, V_{\rm gs}$ high-energy tails of the DFs are less populated in longer MOSFETs, cf. Fig. 12. As a consequence, the contribution of the AB-process becomes less prominent while the relative role of the MVE-process increases. Due to the same reason, since the AB-mechanism is dominant at short stress times, the MVE-process contributes in HCD at longer stress times. Ignoring the effect of the MVE-mechanism leads to a discrepancy which is most pronounced between the transistor source and center. Near the drain carriers are hot enough and bond dissociation events are predominantly triggered by solitary carriers without pre-heating of the bonds by the MVE-process. This is not the case in the rest of the device where excitation of bond vibrational modes becomes more important.

As for the activation energy dispersion, ignoring this ingredient leads

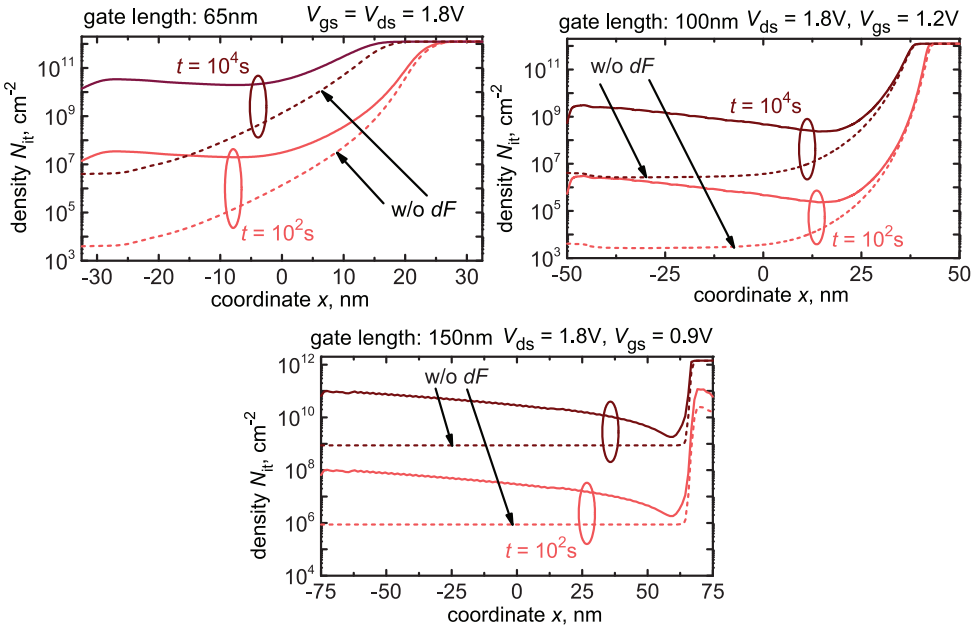

Fig. 13. The interface states density $N_{\rm it}(x)$ profiles plotted for all devices stressed under $V_{\rm ds} = 1.8$V for 100 s and 10 ks considering and ignoring the effect of the activation energy reduction due to the interaction of the electric field with the dipole moment of the bond. In all cases the $d \times E_{\rm ox}$ reduction leads to a secondary $N_{\rm it}$ peak located near the source. The position of this peak coincides with the position of the electric field maximum. If the $d \times E_{\rm ox}$ effect is not considered, the $N_{\rm it}(x)$ profiles are flat in the source section (source is in the left) of the device and correspond to the saturated MVE-mechanism. The source position corresponds to $x =$ -32.5, -50, and -75 nm for the 65, 100, and 150 nm n-MOSFETs, accordingly.

to substantial underestimation of $\Delta I_{\rm dlin}$ observed in the entire stress time slot, see Fig. 10. This is also confirmed by the $N_{\rm it}(x)$ profiles. One can see that the drain $N_{\rm it}$ maximum is almost not affected by the activation energy dispersion. This is because in the drain region of the device carriers are rather hot, the AB-process is saturated, and hence a further reduction of the activation energy does not substantially impact the bond-breakage kinetics in this transistor section.

4.4 The role of electron-electron scattering

The previous results show that the effect of electron-electron scattering can be strong or weak in the same device subjected to various combinations of voltages Fig. 10. Thus, in the case of the 150 nm MOSFET the contribution of electron-electron scattering can be neglected when the device is stressed

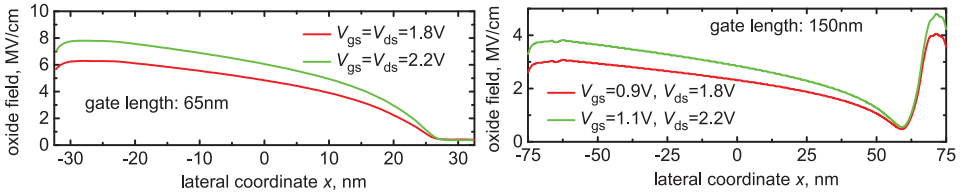

Fig. 14. The electric field profiles evaluated for the 65 and 150 nm n-MOSFETs for both combinations of stress voltages. One can see that in all cases the electric field peaks near the source which leads to a secondary maximum observed in N_{it} profiles at the same position. The source position corresponds to x = -32.5 and 75 nm for the 65 and 150 nm n-MOSFETs, accordingly.

at $V_{gs} = 0.9\,\mathrm{V}$ and $V_{ds} = 1.8\,\mathrm{V}$, while the EES contribution is stronger if the applied voltages are higher: $V_{gs} = 1.1\,\mathrm{V}$ and $V_{ds} = 2.2\,\mathrm{V}$. This trend hints that rather than the gate/channel length alone a superposition of the device architecture and stress conditions is important.

To check this idea we have virtually fabricated a series of n-MOSFETs (using the Sentaurus Process simulator) by the same process flow as 65, 100, and 150 nm transistors but with gate lengths covering a wider range. We used devices with L_G = 44, 200, and 300 nm. According to the work by Rauch *et al.* [28, 29], EES starts to play an important role when the channel length is below 70-100 nm, just within the range used in this work.

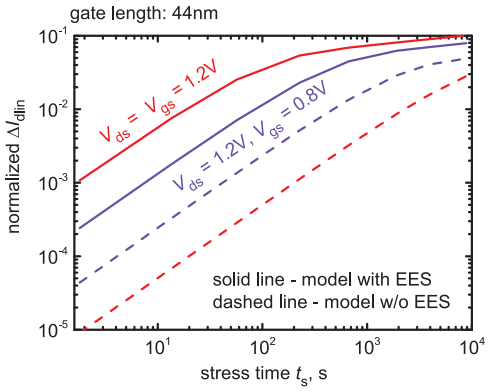

Fig. 15. The normalized linear drain current change simulated for the n-MOSFET with a gate length of 44 nm for two stress conditions: for $V_{gs} = 0.8\,\mathrm{V}$, $V_{ds} = 1.2\,\mathrm{V}$ and for $V_{gs} = V_{ds} = 1.2\,\mathrm{V}$ with and without EES. One can see that in both cases EES plays an important role.

Fig. 15 shows the relative change of the linear drain current plotted as a function of stress time for the 44 nm n-MOSFET simulated with and without electron-electron scattering for $V_{gs} = 0.8\,\mathrm{V}$, $V_{ds} = 1.2\,\mathrm{V}$ and for $V_{gs} = V_{ds} =$

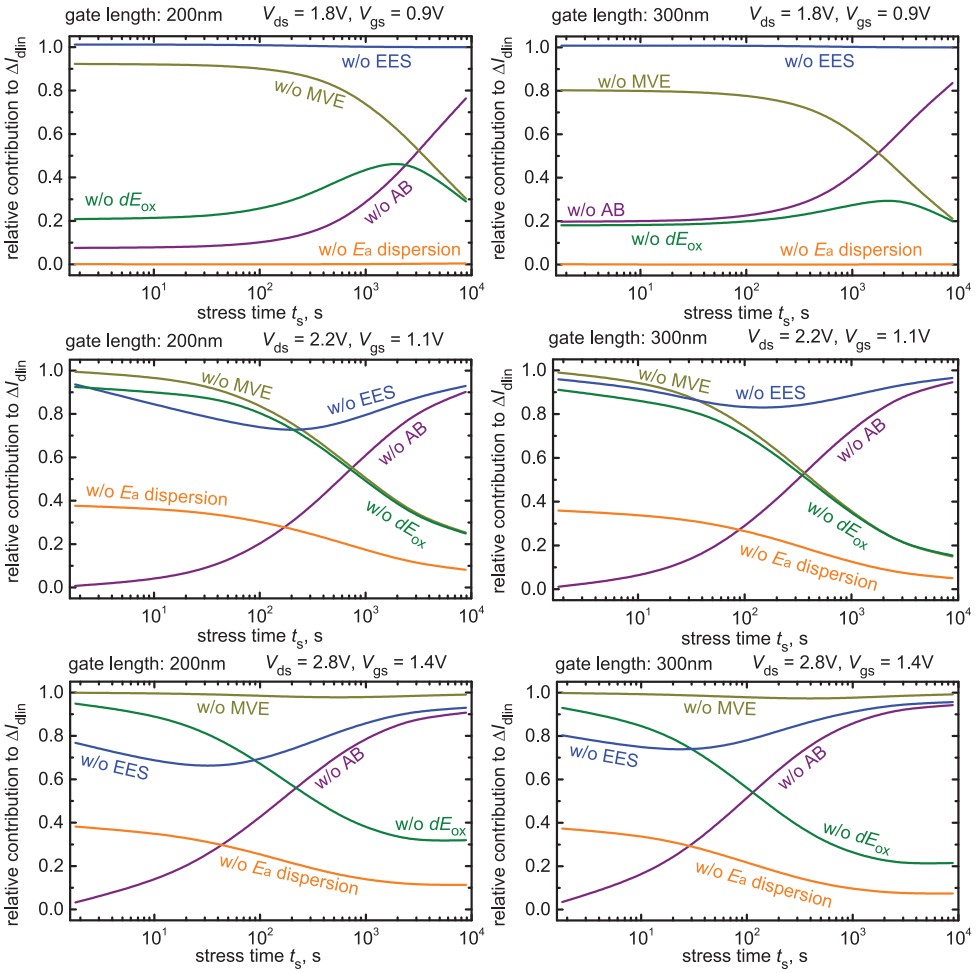

Fig. 16. The ratios between ΔI_{dlin} calculated neglecting one of the model components to that computed with the "full" model obtained for two transistors with $L_{\mathrm{G}} = 200$ and 300 nm for their worst-case conditions and three different drain voltages: $V_{\mathrm{ds}} = 1.8$, 2.2, and 2.8 V.

1.2 V, One can see that even at low voltages as $V_{\mathrm{gs}} = 0.8$ V, $V_{\mathrm{ds}} = 1.2$ V the role of EES is prominent and this mechanism cannot be ignored.

Further, for the 200 and 300 nm devices we plot the relative contribution of the model ingredients, i.e. we analyze the ratios between ΔI_{dlin} computed neglecting one of the model components and that obtained with the "full" model. Fig. 16 depicts these ratios for the worst-case HCD conditions typical for these devices ($V_{\mathrm{gs}} = V_{\mathrm{ds}}/2$) and three different values of the drain voltage: $V_{\mathrm{ds}} = 1.8$, 2.2, and 2.8 V. One can see that the EES effect can be

neglected at low drain voltages ($V_{\mathrm{ds}} = 1.8\,\mathrm{V}$) in both devices. At higher V_{ds}, however, EES starts to play a significant role. For instance, neglecting EES in the 200 nm MOSFET stressed at $V_{\mathrm{ds}} = 2.2$ and 2.8 V leads to a severe ΔI_{dlin} underestimation of more than 20% and 30%, respectively in the time slot of 10-100 s. In the 300 nm counterpart the contribution of EES is less pronounced but still prominent. Thus, if $V_{\mathrm{ds}} = 2.8\,\mathrm{V}$, a discrepancy between $\Delta I_{\mathrm{dlin}}(t)$ curves simulated with and without EES will be more than 25%.

To summarize, the analysis of EES over a wide range of gate lengths (we used $L_{\mathrm{G}} = 44$, 65, 100, 150, 200, and 300 nm) and different combinations of applied voltages suggests that only a consistent consideration of the device topology and stress conditions allows us to judge whether EES is important or not.

5 Conclusions

We have presented and validated a new version of our physics-based model for hot-carrier degradation. Within our model three main levels relevant for HCD are covered and linked, namely the microscopic level of defect generation, carrier transport, and modeling of the degraded devices. The carrier transport kernel is realized using the deterministic Boltzmann transport equation solver ViennaSHE, which incorporates full-band effects and various scattering mechanisms, in particular the electron-electron interaction. The model consolidates such important ingredients relevant for hot-carrier degradation as the two competing mechanisms of Si-H bond dissociation, electron-electron scattering, the reduction of the bond-breakage activation energy due to the interaction of the dipole moment of the bond with the electric field, and statistical fluctuations of this energy.

Our model was validated against HCD experimental data obtained from three n-MOSFETs of an identical architecture but with different gate lengths of 65, 100, and 150 nm. The devices were stressed at their HCD worst-case conditions and two different drain voltages, namely at $V_{\mathrm{ds}} = 1.8$ and 2.2 V. In all cases the model was able to successfully represent the relative linear drain current shift using a unique set of parameters. In order to analyze the importance of each of the model ingredients, $\Delta I_{\mathrm{dlin}}(t)$ curves obtained disregarding one of these ingredients were also evaluated.

We have shown that even in as short devices as n-MOSFETs with a gate length of 65 nm the bond-dissociation process triggered by a solitary hot carrier can play a dominant role when the transistor is stressed at a high voltage (e.g. at $V_{\mathrm{ds}} = 1.8\,\mathrm{V}$). Quite intriguingly, the multiple vibrational excitation

bond-breakage mechanism tends to be more important in longer transistors. At a first glance, this result contradicts the commonly used idea that in short-channel devices HCD is dominated by the MVE-process, while the AB-mechanism drives hot-carrier degradation in long-channel counterparts. Our findings can be understood in the context of the carrier distribution functions. If a combination of $V_{\mathrm{gs}}, V_{\mathrm{ds}}$ is fixed and DFs calculated for MOSFETs with different channel lengths are compared, one concludes that the high energetical fraction of the carrier ensemble is less populated in longer devices under the same voltages. As a result, the relative contribution of the AB-process decreases while the role of the MVE-mechanism increases. The same argument explains why the role of electron-electron scattering becomes less important in longer MOSFETs. As for the interaction of the electric field with the dipole moment of the bond, this effect leads to a secondary maximum observed in N_{it} profiles near the source. This maximum becomes more pronounced with stress time and determines long-term HCD. Neglecting the activation energy dispersion leads to a severe ΔI_{dlin} underestimation within the entire stress time window.

To analyze the role of EES in more detail a series of transistors of the same architecture but with gate lengths of 44, 200, and 300 nm was used. It was shown that in the case of the 44 nm device the EES contribution is prominent even at such low voltages as $V_{\mathrm{gs}} = 0.8\,\mathrm{V}$ and $V_{\mathrm{ds}} = 1.2\,\mathrm{V}$. As for the 200 nm MOSFET, EES can be neglected in the case of $V_{\mathrm{gs}} = 0.9\,\mathrm{V}$ and $V_{\mathrm{ds}} = 1.8\,\mathrm{V}$. However, electron-electron scattering appears to be very important if $V_{\mathrm{gs}} = 1.4\,\mathrm{V}$ and $V_{\mathrm{ds}} = 2.8\,\mathrm{V}$, i.e. ΔI_{dlin} calculated without EES is lower by more than 30% than that obtained with the effect of EES. In the 300 nm counterpart neglecting EES leads to a more than 20% underestimation of ΔI_{dlin} at $V_{\mathrm{gs}} = 1.4\,\mathrm{V}$ and $V_{\mathrm{ds}} = 2.8\,\mathrm{V}$. These findings suggest that rather than the channel/gate length alone a combination of the device architecture and stress conditions is needed to judge on the importance of electron-electron scattering.

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