Comparison of Pulse Width Modulation Techniques for Diode-Clamped and Cascaded Multilevel Inverters

Kishor Gudipati
E.E.E Department, G.Pulla Reddy Engineering College, India
gudipatikishor@gmail.com (corresponding author)

Harsha Vardhan Reddy Maramreddy
E.E.E Department, G.Pulla Reddy Engineering College, India
maramreddyharsha@gmail.com

Sri Gowri Kolli
E.E.E Department, G.Pulla Reddy Engineering College, India
gowrivasu.3@gmail.com

Vuyyuru Anantha Lakshmi
E.E.E Department, G.Pulla Reddy Engineering College, India
v.al@rediffmail.com

Girireddy Sreenivasa Reddy
E.E.E Department, G.Pulla Reddy Engineering College, India
nivasa7hills@gmail.com

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ABSTRACT

Multilevel inverter technology has become the most significant method of energy conversion from DC to AC for uninterrupted power supply. The quality of the power supply depends on the appearance of harmonics, which is considered a problem that needs to be overcome. This paper demonstrates the use of a new modulation technique to reduce the harmonics in both diode-clamped and cascaded multilevel inverters, examining its Total Harmonic Distortion (THD) compared to other PWM methods. Simulations were carried out in MATLAB/Simulink for five-level diode-clamped and cascaded multilevel inverters. The simulation results of both multilevel inverters using the sinusoidal PWM, modified reference PWM, modified carrier PWM, and modified reference and modified carrier PWM methods showed that the latter had the best THD performance for both inverter types, especially for the cascaded multilevel inverter.

Keywords-Harmonics; Multi Level Inverter (MLI); Pulse Width Modulation (PWM)

I. INTRODUCTION

The rapidly expanding field of multilevel power conversion technology in power electronics offers great potential for development. A new breed of multilevel inverters has emerged as a possible alternative to handle high voltage levels. The appropriate multilevel inverter for each application is not always obvious, as it depends on several agile methodologies. Multilevel inverters (MLIs) bring the output waveform closer to a sinusoidal waveform, minimizing Total Harmonic Distortion (THD). Core inverter designs include flying capacitor cascaded and diode-clamped circuits to get beyond the solid-state switching device rating restrictions and facilitate the adoption of multilevel inverter topologies in higher-voltage systems. A design feature of multiple voltage source inverters enables them to achieve high voltages with low harmonics without relying on transformers. The primary function of a multilayer inverter is to combine many layers of DC voltages to produce the desired AC voltage. Table I shows that to accomplish the same number of voltage levels, inverters need an equal number of main switches and main diodes. As cascaded inverters do not require clamping diodes, they have the smallest component count [1-12].

TABLE I. SWITCHES FOR DIFFERENT MULTILEVEL INVERTERS

Types of switches	Diode clamped MLI	Capacitor clamped MLI	Cascaded MLI
Clamping diodes	(n-1)*(n-2)	0	0
Balancing capacitors	0	(n-1)*(n-2)/2	0
Main diodes	2(n-1)	2(n-1)	2(n-1)
DC bus capacitors	(n-1)	(n-1)	(n-1)/2
Main switching devices	2(n-1)	2(n-1)	2(n-1)

II. DIFFERENT MULTILEVEL TECHNIQUES

A. Diode Clamped Inverter (DCMLI)

In a DCMLI, the diode acts as the clamping device to reach stages in the o/p voltage, which makes it a unique MLI when compared with other topologies. In an *m*-level diode-clamped inverter, the voltage over each capacitor is V_{dc}/m-1. The phases are connected to a number of capacitors via the diode-clamped inverter, which produces multiple voltage levels, whether or not each action-switching device prevents V_{dc}/m-1 [13-23].

B. Cascaded Multilevel Inverter (CDMLI)

The flexibility of this arrangement facilitates maintenance and provides a straightforward method of system redundancy. CDMLI is a combination of *H*-bridges that are connected in series. An *N*-level *H*-bridge MLI has two (*N*-1)/2 switches, which are series-connected phases. A single phase makes up each cell. Therefore, the requirement is four active switches in each cell, which can generate three voltage levels: 0, *Vdc*/2, and –*Vdc*/2. Attaching all cells in a cascade will result in voltage stages, with the cell voltages added together making up the phase voltage $V_{an}=V_1+V_2+V_3+\ldots+V_n$ [24-31].

III. DIFFERENT MODULATION TECHNIQUES

There are several different types of modulation techniques to generate pulses to trigger the switches of an inverter.

A. Sinusoidal Pulse Width Modulation (SPWM)

In SPWM, a high switching frequency carrier wave signal, i.e., a triangular wave signal, is compared with the reference sinusoidal signal.

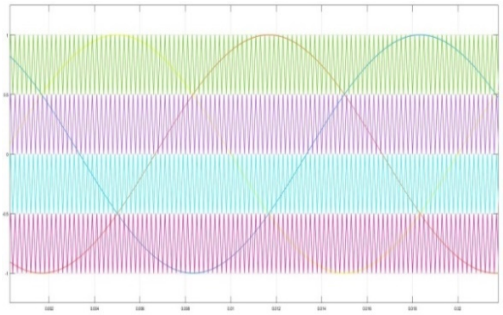

Fig. 1. Sinusoidal reference comparison with normal triangular waves.

SPWM modulates one sinusoidal signal with many triangular carrier signals [32-46]. The carriers' peak-to-peak amplitudes (A_c) and frequencies (F_c) are identical. The zero references of the carrier set are situated in the middle. A switch is triggered if the modulating signal is greater than the triangle carrier assigned to it [47].

B. Modified Reference Pulse Width Modulation (MRPWM)

In the general sinusoidal PWM approaches, for example at 2-level inverters, every phase voltage is set parallel to that of the triangular carrier signal, to generate the voltages [48]. To get the maximum of the common-mode voltage, $V_{offset1}$ is connected to the phase voltages [49-50], therefore:

$$V_{offset1} = \frac{-(V_{max}+V_{min})}{2} \quad (1)$$

While a reference phase voltage is measured throughout a sample, three recommended phase voltages are measured within a sampling time. V_{max} is the voltage at the maximum point and V_{min} is the voltage at the minimum point. When the commons mode voltage, $V_{offset1}$, is included, the effective inverter switching vectors are minimal in a sample period.

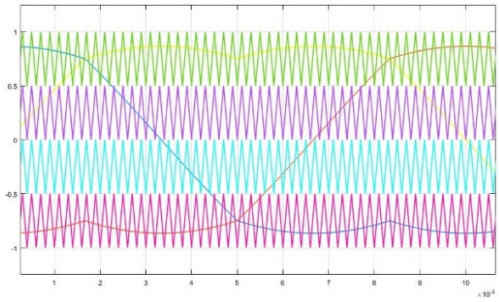

Fig. 2. Modified reference comparison with normal triangular waves.

C. Modified Carrier Pulse Width Modulation (MCPWM)

Figure 3 shows the carrier vertical offset for MLI using the modified carrier technique.

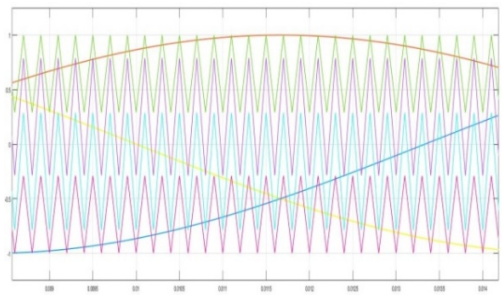

Fig. 3. Sinusoidal reference comparison with modified carrier waves.

The source sine wave is positioned in the center of the four triangular carriers, which can be observed to be overlapped. Each triangular wave is compared with the reference signal and, hence, the triggering pulses are generated.

D. Modified Reference and Modified Carrier Pulse Width Modulation (MRCPWM)

Figure 4 shows the carrier vertical offset MLI using the modified reference and modified carrier technique. The four carriers may be observed to be overlapping, and a modified sine wave (or third harmonic wave) is positioned in the middle

of the four. Each triangular wave is compared with the reference signal and, hence, the triggering pulses are generated.

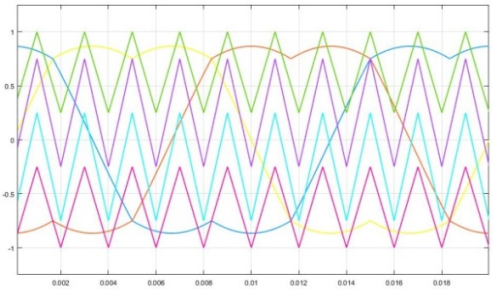

Fig. 4. Modified reference comparison with modified carrier waves.

IV. SIMULATION RESULTS FOR DIODE-CLAMPED MLI

A. Sinusoidal PWM (SPWM)

Figures 5 and 6 show the line voltages and the FFT analysis obtained from a diode-clamped five-level inverter using the SPWM technique to trigger its switches. The obtained THD percentage was 18.09%.

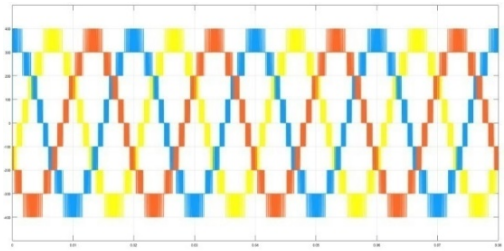

Fig. 5. Line voltages of diode-clamped MLI with SPWM.

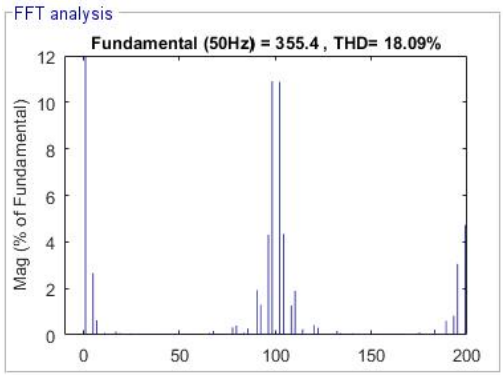

Fig. 6. FFT analysis of diode-clamped MLI with SPWM.

B. Modified Reference PWM (MRPWM)

Figures 7 and 8 show the line voltages and the FFT analysis obtained from a diode-clamped five-level inverter using the MRPWM technique to trigger its switches. The obtained THD was 13.20%, which was lower than the obtained for the same inverter with SPWM.

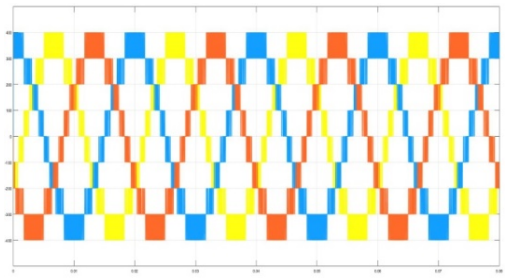

Fig. 7. Line voltages of diode-clamped MLI with MRWM.

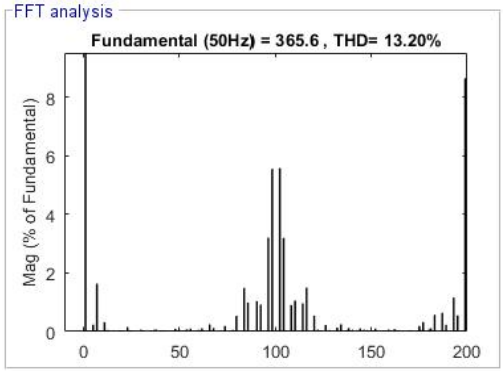

Fig. 8. FFT analysis diode-clamped MLI with MRWM.

C. Modified Carrier PWM (MCPWM)

Figures 9 and 10 show the line voltages and the FFT analysis obtained from the diode-clamped five-level inverter using the MCPWM technique to trigger its switches. The obtained THD was 11.10%, which was lower than those obtained for the same MLI type with SPWM and MRPWM.

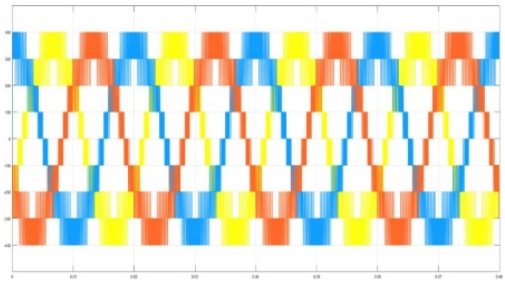

Fig. 9. Line voltages of diode-clamped MLI with MCPWM.

D. Modified Reference and Modified Carrier PWM (MRMCPWM)

Figures 11 and 12 show the line voltages and the FFT analysis obtained from the diode-clamped five-level inverter using the MRMCPWM technique to trigger its switches. The obtained THD was 10.22%, which was lower than those obtained for the same type of MLI with the other techniques.

V. SIMULATION RESULTS FOR CASCADED MLI

A. Sinusoidal PWM (SPWM)

Figures 13 and 14 show the line voltages and the FFT analysis obtained for the cascaded five-level inverter using the

SPWM technique to trigger its switches. The percentage of THD obtained was 17.47%. As this PWM technique for the diode-clamped MLI obtained 18.09% THD, this technique worked better for cascaded MLI.

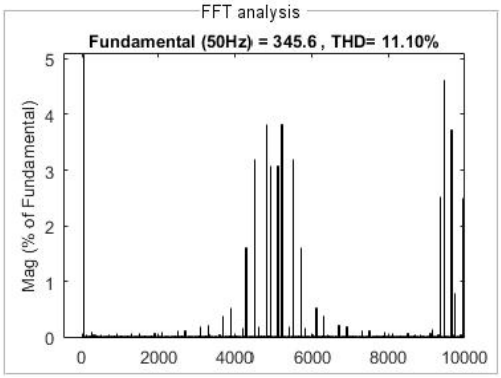

Fig. 10. FFT analysis of diode-clamped MLI with MCPWM.

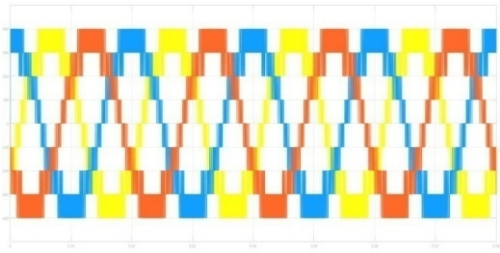

Fig. 11. Line voltages of diode-clamped MLI with MRMCPWM.

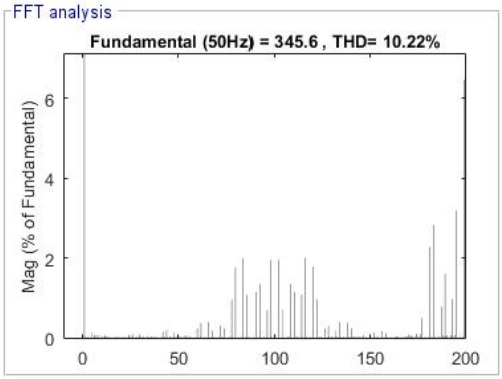

Fig. 12. FFT analysis of diode-clamped MLI with MRMCPWM.

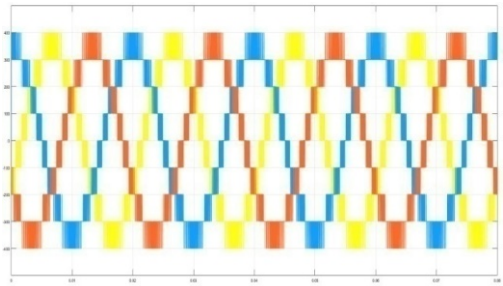

Fig. 13. Line voltages of cascaded MLI for SPWM.

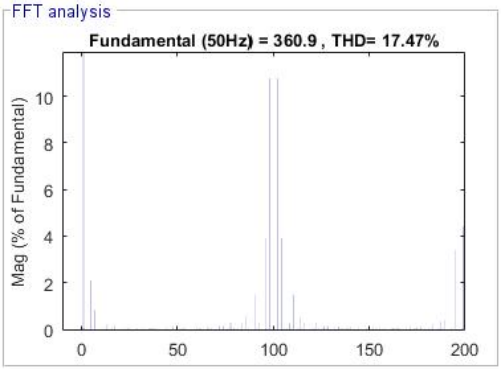

Fig. 14. FFT analysis of cascaded MLI for SPWM.

B. Modified Reference PWM (MRPWM)

Figures 15 and 16 show the line voltages and the FFT analysis obtained for the cascaded five-level inverter using the MRPWM technique to trigger its switches. The THD obtained was 13.08%, showing that this technique also worked better for cascaded MLI.

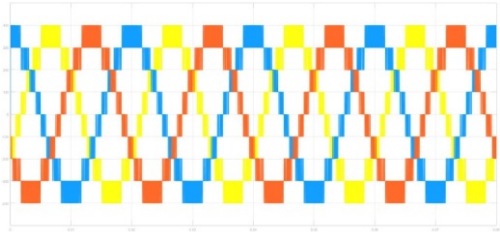

Fig. 15. Line voltages of cascaded MLI with MRPWM.

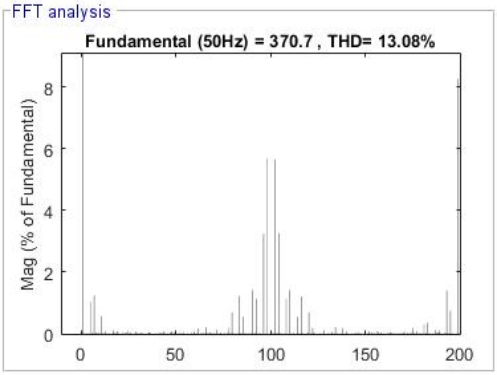

Fig. 16. FFT analysis of cascaded MLI with MRPWM.

C. Modified Carrier PWM (MCPWM)

Figures 17 and 18 show the line voltages and the FFT analysis obtained for the cascaded five-level inverter using the MCPWM technique to trigger its switches. The THD obtained was 11.05%.

D. Modified Reference and Modified Carrier PWM (MRMCPWM)

Figures 19 and 20 show the line voltages and the FFT analysis obtained for the cascaded five-level inverter using the

MRMCPWM technique to trigger its switches. The THD obtained was 10.14%, which is smaller compared to the result when using the same PWM technique for the diode-clamped MLI. Therefore, this technique works better for cascaded MLI.

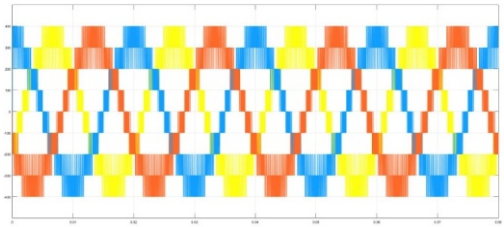

Fig. 17. Line voltages of cascaded MLI with MCPWM.

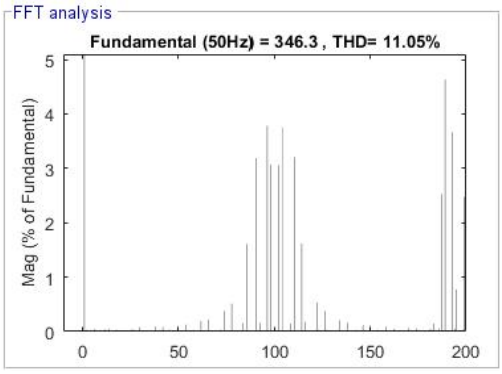

Fig. 18. FFT analysis of cascaded MLI with MCPWM.

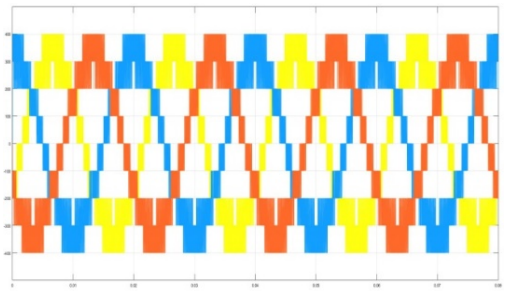

Fig. 19. Line voltages of cascaded MLI with MRMCPWM.

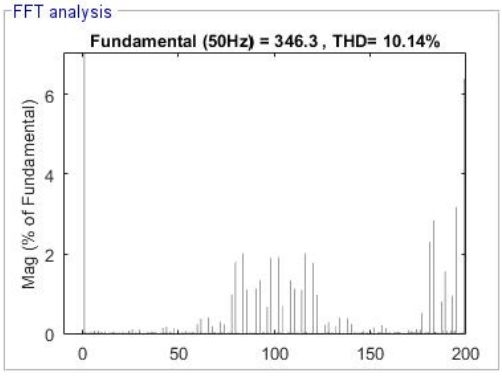

Fig. 20. FFT analysis of cascaded MLI with MRMCPWM.

VI. RESULTS AND DISCUSSION

Table II demonstrates the performance of the diode-clamped multilevel inverter in terms of THD using the SPWM, MRPWM, MCPWM, and MRCPWM techniques. This table clearly shows that of all the mentioned PWM techniques, the MRCPPWM technique worked better, as its THD percentage was lower. The lower the THD percentage, the higher the quality of power delivered by the inverter.

TABLE II. DCMLI THD RESULTS

DCMLI (Diode Clamped Multilevel inverter)				
Switching frequency(Hz)	**Sinusoidal PWM (% THD)**	**MRPWM (%THD)**	**MCPWM (%THD)**	**MRCPWM (%THD)**
1KHz	23.54	18.40	16.2	14.13
5KHz	20.01	15.14	13.0	11.12
10KHz	18.09	13.20	11.1	10.22

Table III demonstrates the performance of cascaded MLI in terms of THD using SPWM, MRPWM, MCPWM, and MRCPWM. This table clearly shows that of all the mentioned PWM techniques, the MRMCPWM worked the best, as its THD percentage was lower for the cascaded MLI. The cascaded MLI is a widely used inverter where a small decrease in its THD makes the inverter suitable for wide applications. The power quality obtained by lowering the THD percentage in cascaded MLI can fill the gap in many power quality issues.

TABLE III. CDMLI(CASCADED MULTILEVEL INVERTER)

CDMLI (Cascaded Multilevel inverter)				
Switching frequency(Hz)	**Sinusoidal PWM (% THD)**	**MRPWM (% THD)**	**MCPWM (% THD)**	**MRCPWM (% THD)**
1KHz	23.00	18.30	16.0	13.92
5KHz	19.89	14.52	12.7	11.01
10KHz	17.47	13.08	11.0	10.14

Table IV demonstrates the THD of both the cascaded multilevel and the diode-clamped inverters using MRMCPWM. The results show that the MRMCPWM is the best PWM technique compared to conventional PWM techniques. Moreover, the higher the switching frequency, the lower the harmonics were observed for both inverter topologies. The lower harmonics in the power supply improved power quality, which affects the torque produced in motor drives. Furthermore, the efficiency and life span of any motor drive is directly proportional to the quality of the power supplied to it.

TABLE IV. MODIFIED REFERENCE AND MODIFIED CARRIER PWM (MRCPWM)

Switching frequency(Hz)	**Diode clamped MLI (THD in %)**	**Cascaded MLI (THD in %)**
1KHz	13.92	13.45
5KHz	11.12	11.01
10KHz	10.22	10.14

It should be noted that for both inverters with different PWM techniques, a resistive load of 10Ω was taken, the modulation index was 0.8, and the DC link voltage was 400V.

VII. CONCLUSION

This study presented the harmonic spectrum for cascade and diode-clamped 3-phase 5-level inverters using the SPWM, MRPWM, MCPWM, and MRMCPWM techniques. A comparison of these techniques for both inverters showed that MRCPWM provided a spectrum that is tolerant for application, especially for the cascaded MLI inverter. Therefore, for any five-level inverter application, it is recommended to use the MRCPWM technique as its THD percentage is significantly lower.

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