A Review on Energy Efficient CMOS Digital Logic

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Abstract— **Autonomy of power supply used in portable devices directly depends on energy efficiency of digital logic. This means that digital systems, beside high processing power and very complex functionality, must also have very low power consumption. Power consumption depends on many factors: system architecture, technology, basic cells topology-speed, and accuracy of assigned tasks. In this paper, a review and comparison of CMOS topologies techniques and operating modes is given, as CMOS technology is expected to be the optimum choice in the near future. It is shown that there is a full analogy in the behavior of digital circuits in sub-threshold and strong inversion. Therefore, synthesis of digital circuits is the same for both strong and weak operating modes. Analysis of the influence of the technology, MOS transistor threshold voltage (V_t) and power supply voltage (V_{dd}) on digital circuit power consumption and speed for both operating modes is given. It is shown that optimal power consumption (minimum power consumption for given speed) depends on optimal choice of threshold, and power supply voltage. Multi V_{dd}/V_t techniques are analyzed as well. A review and analysis of alternative logical circuit's topologies – pass logic (PL), complementary pass logic (CPL), push-pull pass logic (PPL) and adiabatic logic – is also given. As shown, adiabatic logic is the optimum choice regarding energy efficiency.**

Keywords: topology; technology; power consumption; logic delay; CMOS; strong and weak inversion; static and dynamic characteristics; pass logic; adiabatic logic; PL; CPL; PPL; ECRL

I. INTRODUCTION

Designers of digital circuits are confronted with two often conflicting demands: how to achieve higher operating speeds and lower energy consumption. Usually, the same circuit family could not satisfy both demands at the same time, i.e. high-speed circuits have high level of consumption and vice versa. That's how series of integrated circuits called low-power circuits or high-speed circuits were created. Optimally designed digital system includes a variety of different series of the same integrated circuits' family.

Today, as the whole digital system is manufactured as a single integrated circuit, the designing problem is reduced to the choice of a design that can ensure maximum energy efficiency. That implies the design with minimum power consumption inside the specified frequency range or maximum operating speed for a given energy consumption level. The usage of low-power sources of power supply, which collect their primary energy from the environment, has increased lately. Thus, the art of design of low power circuits is brought down to the selection of optimal (intelligent) solutions that will reduce the speed of information processing as much as possible, without violating certain system characteristics. Such an optimal project implies the decomposition of the system architecture, good choice of the circuit topology that will provide the optimal synthesis of different functions in the defined architecture, and good choice of the circuit design technology. This requires the designer to be familiar with components, circuits and systems. Consumption of each system is determined using the following five guidelines of each project: given task, technology, circuit topology, operating speed and accuracy. Since these five guidelines can be placed on the fingers of one hand, they are known as "low-power hand" [1]. Therefore, optimization of energy consumption is a multidimensional problem that requires taking into consideration the level of consumption at each stage of the VLSI integrated circuit design. The biggest savings of electrical energy consumption (10 to 20 times), with least waste of time (at the level of a minute) is done in the early stages of designing, in which the project is presented as a set of abstract communication tasks [2]. The application of optimization techniques and consumption provides an estimation at each project stage, leading to optimal consumption project [3]. At lower levels of the design (transistor, deployment and connectivity), possible energy savings are significantly lower (10 to 20%), and time estimation can last for days, because the project is presented with all detail. Thus, it is necessary to process a very large amount of data [3]. CMOS digital circuits' technology based on silicon will most likely be dominant for the next twenty years or more [4, 5, 6], with standard low power consumption, technology for reducing the transistor size to a scale of about ten nanometers and operating speed in the GHz domain. During the last ten years, more attention from researchers as well as manufacturer of integrated circuits is paid to digital CMOS circuits operating in the sub-threshold (weak inversion) regime. Supply voltage in this regime is lower than the threshold voltage V_t of MOS transistors ($V_{dd}<V_t$) and is about a few hundred millivolts. Thanks to that fact, the dynamic consumption level is significantly reduced in regard to CMOS circuits operating in the strong inversion regime. Since the operating area in the sub-threshold regime is overlapped with the area of a disconnected transistors in strong inversion regime, current ratio in on and off the state has been significantly reduced. Consequently, CMOS circuit logic delay

in the sub-threshold regime is several orders of magnitude higher.

Designers of CMOS digital devices, especially portable ones, have a challenging requirement: how to ensure high processing power and very complex functionality along with low power consumption. Certainly part of the solution is a proper choice of CMOS technology as well as weak and strong inversion regime operating areas.

Although MOS transistor static characteristics in weak inversion and strong inversion regimes are functionally very different, it will be shown that there is an absolute analogy in the behavior and functional dependency of CMOS circuit parameters in those regimes. Thanks to that, design techniques of more complex CMOS circuits are the same in sub-threshold and strong inversion regime. This fact considerably facilitates designer's work of CMOS circuit in a sub-threshold regime and enables faster development.

Optimal consumption generally does not mean minimal consumption. Minimal consumption and minimal logic delay are mutually opposite requirements. Taking into account only the minimization of consumption, a project with unacceptable logic delay could be delivered. The consumption as well as the logic delay of CMOS circuit depends on MOS transistor threshold voltage V_t and supply voltage V_{dd}. Because of that, one part of this paper is devoted to consumption optimization techniques in systems with multiple levels of V_t and V_{dd}.

Specific part of this paper refers to the big toe of "low-power hand"– topologies. Review of topologies of CMOS logic series that ensure low-power within the specified range of operating frequencies is given, which implies their use in both strong and weak inversion regimes.

The analysis is based on simplified current-voltage models of MOS transistors and PSPICE software using parameters of 180 nm technology.

II. CMOS OPERATING IN THE WEAK INVERSION REGIME

In essence, there are three areas of MOS transistor static characteristics [7]. Figure 1 shows the logarithmic dependence of nMOS transistor drain current as a function of gate-source voltage (V_{gs}), at a constant drain-source voltage (V_{ds}) and source-substrate voltage (V_{sb}). In the literature, the smallest attention is paid to the medium (moderate) area which is mostly considered as a part of strong inversion threshold area [8, 9]. In digital circuits, it is assumed that $V_{gs}>V_t$, where V_t is a MOS transistor's threshold voltage, transistor is operating in strong inversion regime, and for $V_{gs}<V_t$ in the sub-threshold (weak inversion) regime. Therefore, from today's application point of view, it can be said that V_t is a gate-source voltage on a border between the weak and the strong inversion regime.

It is a well-known fact that the $I_d(V_{ds}, V_{gs})$ characteristic in the strong inversion regime has two areas: non-saturated and saturated. In the non-saturated area, it holds that $I_d \sim V_{gs}$ and $I_d \sim V_{ds}^2$, while in saturated area $I_d \sim V_{gs}^2$ and $I_d \neq f(V_{ds})$, that is $I_d \approx const$ as a function of V_{ds}.

MOS transistor characteristics in the weak inversion regime are defined as follows:

$$I_{Dsub} = \begin{cases} I_0 e^{\frac{V_{gs}-V_t}{n\varphi_t}} \left(1-e^{-V_{ds}/\varphi_t}\right), V_{ds} < 3\varphi_t, \text{ non-saturated area} \\ I_0 e^{\frac{V_{gs}-V_t}{n\varphi_t}}, V_{ds} > 3\varphi_t, \text{ saturated area,} \end{cases} \quad (1)$$

where

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1)\varphi_t^2 \quad (2)$$

is a drain current on a border between weak and strong inversion.

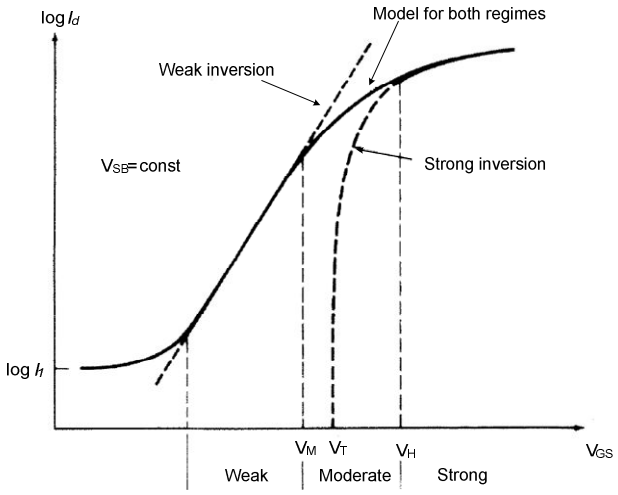

Fig. 1. log I_d characteristic as a function of V_{gs} at a constant V_{ds} and V_{sb}

The meaning of the parameters in (1) and (2) are the following: μ_0 is a mobility of major charge carriers (electrons and holes in nMOS to pMOS transistor), $C_{ox} = \varepsilon_{ox} / t_{ox}$ is gate capacitance (ε_{ox} is a dielectric constant, t_{ox} is a thickness of the gate oxide), W and L are the width and length of the channel, respectively, $\varphi_t=kT/q$ is a thermal potential (φ_t=26 mV at T=300K), where $n=1+C_d/C_{ox}\approx1.5$ is a gradient factor.

For $V_{ds}>3\varphi_t$, drain current is almost independent of the voltage V_{ds} (Figure 2), so that the area analogous to strong inversion regime, can be treated as saturated area. In this area it holds $I_d \sim e^{V_{gs}}$. For $V_{ds}<3\varphi_t$, at $V_{gs}=const.$, $I_d \sim e^{V_{ds}}$, transistor is in the non-saturated area.

Thanks to the analogy in the field of MOS transistor characteristics, there is an appropriate analogy of operation and CMOS logic circuit characteristics [8]. Thus, for example, voltage and current static characteristics in the weak inversion regime (Figure 3) have the same shape as in the strong inversion regime. Even inverter threshold voltage V_{Tsub} is

obtained in the same way – equating of nMOS and pMOS drain currents in the saturated area of characteristics.

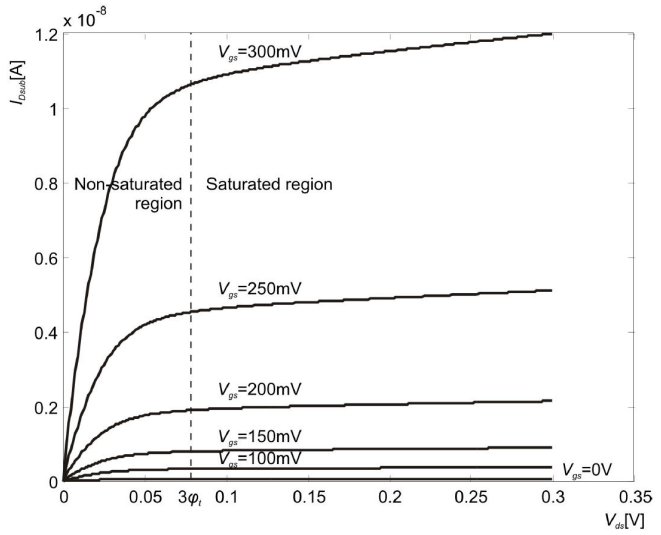

Fig. 2. $I_d(V_{gs}, V_{ds})$ in weak inversion regime

It results with inverter threshold voltage V_{Tsub} in the sub-threshold regime [8]:

$$V_{Tsub} = \frac{V_{ddsub}}{2} - \frac{n\varphi_t}{2}\ln\left(\frac{I_{on}}{I_{op}}\right), \tag{3}$$

and maximal current from the voltage source:

$$I_{ddMsub} = I_{on}\sqrt{\frac{I_{op}}{I_{on}}}e^{\frac{V_{ddsub}/2-V_t}{n\varphi_t}}, \tag{4}$$

where

$$3\varphi_t < V_{ddsub} < V_t = V_{tn} = \left|V_{tp}\right| \tag{5}$$

is a supply voltage, V_{tn} and V_{tp} threshold voltages, and I_{on} and I_{op} currents on the border between weak and strong inversion of nMOS and pMOS transistors, respectively. For a symmetric inverter (I_{on}=I_{op}), threshold voltage is, just like in strong inversion regime, V_{Tsub}=V_{ddsub}/2.

Minimal supply voltage, according to [7] is V_{ddmin}=3φ_t=78 mV. For V_{ddsub}>3φ_t , the $I_d(V_{gs}, V_{ds})$ characteristic has both saturated and non-saturated areas, which is necessary for satisfying the quality of digital circuit transfer characteristic $V_o(V_i)$. However, logic circuits can operate even at V_{dd}<3φ_t. Thus, for example, some authors [9] state constraints V_{dd}>57 mV, while others [10] claim that V_{dd}>48 mV.

As in strong inversion regime, threshold voltage V_{Tsub} and maximal current I_{ddMsub} in the sub-threshold regime both depend on nMOS and pMOS transistor geometry (Figure 3), except that I_{ddMsub}~$(W_n/W_p)^{-1/2}$ and V_{Tsub} ~$ln(W_n/W_p)$, where W_n and W_p are the channel widths of nMOS and pMOS transistors, respectively.

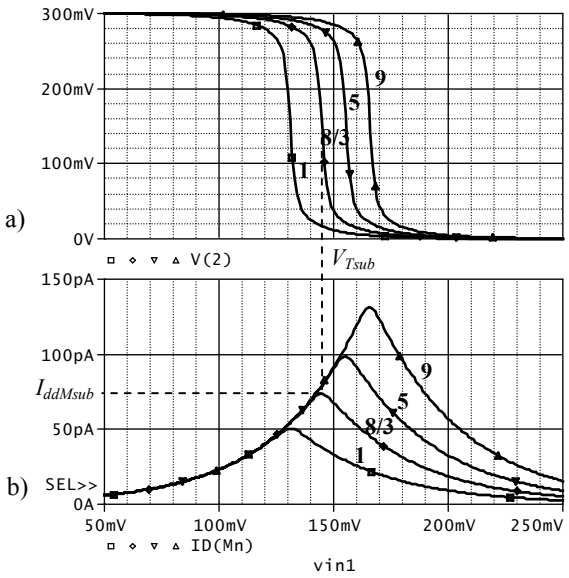

Fig. 3. (a) PSPICE voltage and (b) current transfer characteristic of CMOS inverter in the sub-threshold regime, for channel width ratios W_p/W_n={1, 8/3, 5, 9} at equal channel length (L_n=L_p) and V_{ddsub}= 300 *mV*

Considering the behavior analogy and CMOS inverter characteristics in the weak and strong inversion regime, there is an analogy even at synthesis of more complex circuits. In both regimes, more complex digital circuits consist of dual nMOS and pMOS transistor networks (Figure 4). Duality implies that a serial connection of nMOS transistors is corresponding to a parallel connection of pMOS transistors and vice versa.

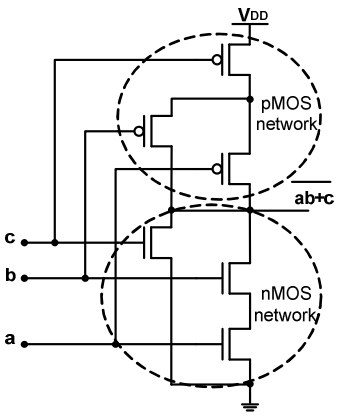

Fig. 4. Topology of the circuit with logical function $\overline{ab+c}$ consisted of dual networks: $ab+c$ (nMOS) and $(a+b)c$ (pMOS)

In both regimes, logic circuit transfer characteristic depends on the number of inputs and number of active inputs [8]. Figure 5a shows the transfer characteristics of NOR3 logic circuit with all inputs activated, and when the activated input is the one applied to the gate of a pMOS transistor whose source is connected on a power-supply line V_{dd}.

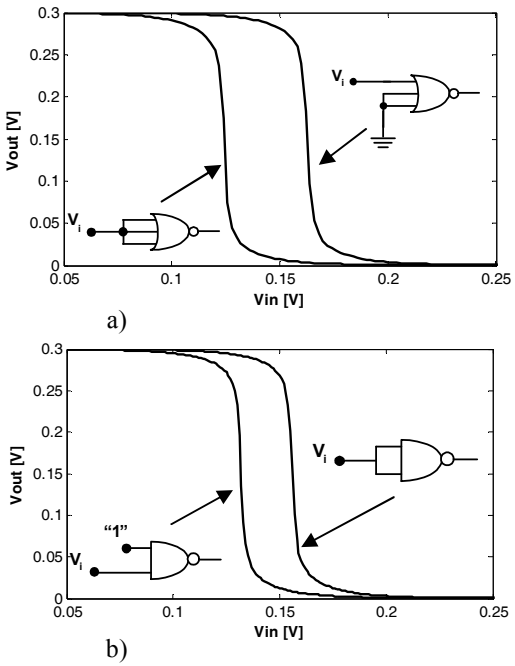

Fig. 5. PSPICE transfer characteristics of (a) NOR3 and (b) NAND2 circuits in the weak inversion regime, with all inputs activated, and when the activated input is the one applied on the gate of a serial transistor whose source connected on power supply line.

In NAND circuits, the highest threshold voltage is obtained when all inputs are active, and the lowest when the active input is only the one applied to the gate of nMOS transistors, whose source is connected to the ground (Figure 5b). Optimal transistor geometry of m-input NAND and NOR circuits is the same in both regimes and is defined as follows [12]:

$$\text{NIm:}\quad \frac{W_n / L_n}{W_p / L_p} = m\frac{\mu_p}{\mu_n} \qquad \text{NILIm:}\quad \frac{W_n / L_n}{W_p / L_p} = \frac{1}{m}\frac{\mu_p}{\mu_n}. \tag{6}$$

III. CMOS CIRCUIT POWER CONSUMPTION

Electric power consumption consists of two components: static and dynamic

$$P_D = P_{DS} + P_{DD}. \tag{7}$$

Static consumption is a result of existing MOS transistor currents in static states and is defined as:

$$P_{DS} = I_S V_{dd}, \tag{8}$$

where I_S represents the static current in total.

There are four main sources of static current in CMOS circuits:

- Tunneling current through the gate (I_g),
- Sub-threshold drain current (I_{dsub}),
- Inverse polarized *p-n* junction current (I_{DSS}),
- Hot charge carrier injection gate current (I_H).

The first three components have dominant influence on CMOS circuit static consumption level.

Scaling of the dimensions of MOS transistors decreases oxide thickness below the gate (t_{ox}). Therefore, the electric field through gate oxide increases, which leads to the tunneling effect of charge carriers from gate to substrate or from substrate to gate. The gate current has four components: gate-channel (I_{gc}), gate-drain (I_{gd}), gate-source (I_{gs}) and gate-base (I_{gb}) (Fig. 6). The total gate current is:

$$I_g = I_{gd} + I_{gb} + I_{gs} + I_{gc}. \tag{9}$$

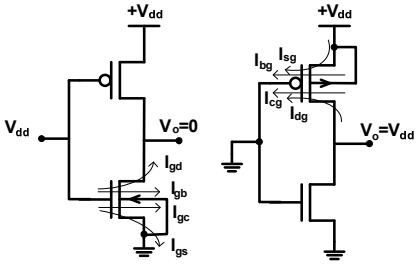

Fig. 6. Gate leakage currents of (a) nMOS and (b) pMOS transistor

Gate currents depend on supply voltage V_{dd} and on the employed technology (Table I) [11]. Thus, for example, when increasing the supply voltage level from V_{dd}=0.2 V to V_{dd}=1.2 V, the gate current increases from $I_g \approx$1.2 nA to $I_g \approx$1.7 μA. The increase ratio is approximately $1.4 \cdot 10^3$ times. When reducing the transistor dimensions, gate current increases as well. For nMOS transistor, according to Table I, that increase for 45 nm in regard to 65 nm CMOS technology, depending on V_{dd}, is approximately 7 (at V_{dd}=1.2 V) to 14 (at V_{dd}=0.2 V) times.

TABLE I. NMOS TRANSISTOR GATE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE FOR TWO DIFFERENT TECHNOLOGIES

V_{dd} [V]	I_g	
	45 nm tech.	65 nm tech.
0.2	1.1996 nA	85.506 pA
0.4	14.258 nA	1.2376 pA
0.6	66.954 nA	6.5488 nA
0.8	225.97 nA	25.244 nA
1.0	647.38 nA	82.378 nA
1.2	1.6811 μA	243.21 nA

The nMOS transistor leakage current is greater than in pMOS, because the probability of holes tunneling is greater than the probability of electrons tunneling through the gate oxide. That increase, depending on supply voltage is 40 times [11].

The sub-threshold leakage current is a cutoff transistor (V_{gs}=0) drain to source current (Figure 7) and it is given as:

$$I_{ddsub} = I_o e^{\frac{\eta V_{dd} - V_t}{n\varphi_t}} \quad (10)$$

where η is the DIBL (Drain–Induced Barrier Lowering) factor [9].

This current values depend on the supply voltage, the dimensions of elements (technology) and the temperature. In Table II, comparative values of gate current and sub-threshold drain current as a function of supply voltage V_{dd} and temperature are given, for 45 nm technology. It is evident that the dependency of I_g on V_{dd} and in function of temperature dependency of I_{dsub} is more expressed. On the other hand, at temperature of 25°C it holds $V_{dd} \leq 0.6$ V, $I_g < I_{dsub}$, while for $V_{dd} > 0.6$ V, $I_g > I_{dsub}$. Thus, for example, for $V_{dd} = 1.2$ V holds that $I_g \approx 13 I_{dsub}$.

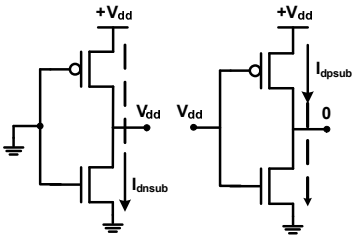

Fig. 7. Sub-threshold currents of (a) nMOS and (b) pMOS transistors in CMOS inverter

TABLE II. GATE AND SUB-THRESHOLD DRAIN CURRENT OF NMOS TRANSISTOR AS A FUNCTION OF V_{DD} AND TEMPERATURE

V_{dd} [V]	Gate current I_g [nA]		Sub-threshold current I_{dsub} [μA]	
	25°C	110°C	25°C	110°C
0.2	1.1996	1.2689	40.999	0.88086
0.4	14.258	15.776	56.437	1.1586
0.6	66.954	75.437	72.47	1.4401
0.8	225.97	256.33	89.397	1.7334
1.0	647.38	736.31	107.42	2.0428
1.2	1681.1	1914.3	127.12	2.3785

Inverse saturation current Idss of the p-n junction of a turned off transistor depends on the *p-n* junction surface and temperature. For 0.25 μm technology, it is between 10 and 100 pA/μm^2 at a 25°C temperature per area unit. In nanometer technologies, this current is less than I_g and I_{dsub}, and can be ignored.

Dynamic consumption consists of two components: switching consumption and transition (short-circuits) consumption. Switching consumption is the result of charging and discharging of a load capacitor and in both regimes is defined as:

$$P_d = P_{ddsub} = C_L V_{dd}^{\ 2} f, \quad (11)$$

where C_L is the effective output parasite capacitance, and f is the switching state frequency of the CMOS logic circuit.

Transition consumption occurs due to conduction of both transistors or transistor networks (nMOS or pMOS) during switching states (transition area) (Figure 3). In strong inversion regime, transition consumption is defined with [12] and is:

$$P_{dp} = \frac{1}{3} I_{ddM} \left(V_{DD} - 2V_t\right)\left(t_r + t_f\right) f, \quad (12)$$

where

$$I_{ddM} = \mu_n \frac{C_{ox}}{2} \frac{W_n}{L_n} \frac{\left(V_{DD} - 2V_t\right)^2}{\left(1 + \sqrt{\frac{\mu_n}{\mu_p} \frac{W_n / L_n}{W_p / L_p}}\right)^2} \quad (13)$$

is the maximal voltage supply current in transition area, and t_r and t_f are the rise time and fall time input signals.

In sub-threshold regime, dissipation power of transition is defined with [8] :

$$P_{dpsub} = 2n\varphi_t I_{ddMsub} \left(t_r + t_f\right) f, \quad (14)$$

where I_{ddMsub} is defined with (4), and f is an input signal frequency.

Usually, dynamic dissipation power is calculated (estimated) in regard to clock frequency. Namely, most number of logic circuits does not change their state during every cycle of clock signal. Therefore, expressions for dynamic consumption have to be multiplied with activity factor $\alpha \leq 1$, regarding to clock frequency, so that:

$$P_{dd} = \alpha f_c C_L V_{dd}^{\ 2} + \alpha f_c \frac{I_{ddM}}{3} \left(V_{dd} - V_t\right)\left(t_r + t_f\right),$$
$$P_{ddsub} = \alpha f_c C_L V_{ddsub}^{\ 2} + \alpha f_c 2n\varphi_t I_{ddMsub} \left(t_r + t_f\right). \quad (15)$$

Product αf_c, where f_c is the clock frequency, is the activity of the circuit indicating the number of state changes. Mostly, activity factor is $\alpha < 0.5$. It is determined empirically that static CMOS digital circuits have $\alpha \approx 0.1$ [13].

IV. LOW POWER DESIGN TECHNIQUES

Optimal project implies a compromise between operating speed and low power, which all design levels take into account [2]. In this section, we will speak about the optimal project considering the choice of transistor threshold voltage V_t and system power supply voltage V_{dd}.

In the previous paragraph, it was shown that both static and dynamic consumptions are decreased with the reduce of V_{dd}. Dynamic switching consumption in both regimes is proportional to V_{dd}^2. Transition consumption in the strong inversion regime is $P_{dp} \sim (V_{dd} - V_t)^3$, and in sub-threshold regime $P_{dpsub} \sim e^{V_{dd}/2 - V_t}$. Static currents, depends on supply voltage as well (Tables I and II), so that $P_S \sim V_{dd}^n$, where n is usually in the range of $1 < n < 4$.

Logic delay also depends on V_{dd} and V_t. Namely, in the strong inversion regime, capacitor charging/discharging current is $I_d \sim (V_{dd} - V_t)^2$ in the saturated area, and $I_d \sim (V_{dd} - V_t)V_o$ in the non-saturated area (Figure 8). In the sub-threshold regime that current is $I_{dsub} \sim e^{V_{dd}-V_t} = e^{-(V_t - V_{dd})}$ (Figure 8). Thus, reduction of V_{dd} increases the logic delay in both regimes. In order to maintain the logic delay at lower V_{dd} , threshold voltage V_t should be reduced. Over a long period of time, CMOS digital circuit's performance increasing scenario was conducted in the process of reduction of element's dimensions, by lowering V_{dd} and V_t. However, reduction of V_t below 200 mV leads to exponential increase of sub-threshold current as shown in (4). This may cause the static consumption to be higher than the dynamic. Consequently, it can be said that the reduction of threshold voltage is limited to approximately V_{tmin}=200 mV.

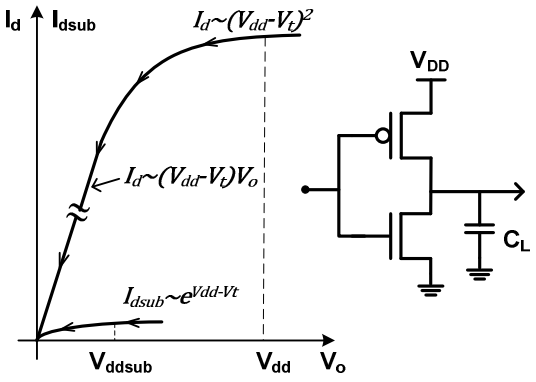

Fig. 8. Discharge currents of capacitor C_L in the strong and weak inversion regime

V. MULTI VDD /VT OPTIMIZATION TECHNIQUES

A compromise between low power and sufficient speed can be achieved using transistors with different threshold voltages. This technique is known as the multi-threshold technique or MTCMOS [14, 15]. Critical signal path is designed using logic with lower threshold voltages. Transistors with higher V_t are used where delay is not critical. The second approach with the MTCMOS technique is based on the so-called gated voltage supply (Figure 9). In static states, relatively in time of logic inactivity (*Standby Mode*), voltage supply is turned off using transistors with high threshold voltage. Thus, the small sub-threshold current is secured, along with low static dissipation. Logic block transistors are designed with low V_t so that the needed speed is preserved.

Using control "wake up" signal $\overline{SL}$ (*Sleep*), over a pMOS transistor with high V_t, the connection between true V_{dd} and virtual power supply V_{ddV} is controlled. While M_p is turned off, capacitor C_B maintains the virtual power supply of the logic block.

Reduction of the leakage currents of inactive components can be achieved using nMOS transistors between the logic block and the ground, or with pMOS and nMOS transistors at the same time [15]. The state of the pMOS transistors is then controlled with the $\overline{SL}$ signal, and of the nMOS with the *SL* signal.

The ratio between the consumption and the speed of data processing is optimized using several power supplies in the same design. Logic circuits over critical delay paths are supplied with higher V_{ddH}, and circuits whose delay is not critical with lower voltage V_{ddL} (Figure 10). The number of voltage levels can be greater, but it turns out that the largest effect is achieved using two power supplies [16]. It should be noted that the transition from logic with V_{ddL} to logic with V_{ddH} power supply is achieved using logic voltage level converters. This as well limits the number of power supply levels.

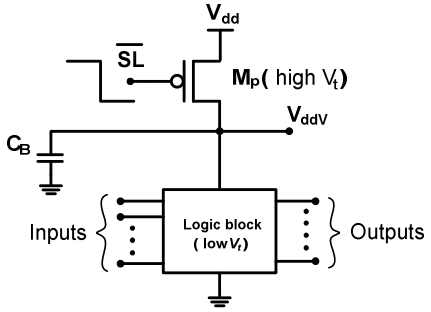

Fig. 9. MTCMOS block diagram with gated voltage supply

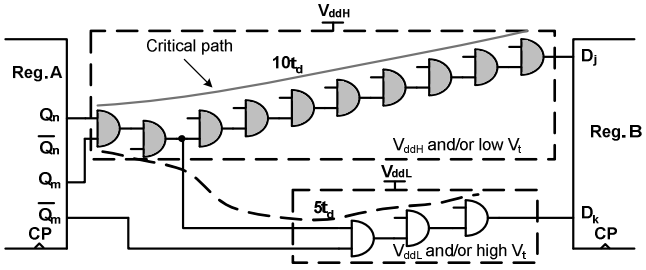

Fig. 10. Two registers connected with different delay paths

Often in the same digital system, techniques with several power supplies and several threshold voltages have been used – multi V_{dd} /V_t techniques [16, 17]. Optimal operating point (V_{ddopt}, V_{topt}) is determined on V_{dd} -V_t plane with constant power consumption lines (*equi-power*) and speed lines (*equi-speed*) (Fig. 11). These lines depend on technological process and project architecture.

The choice of the optimal (V_{ddopt},V_{topt}) pair depends on technological process constraints. Let say that those constraints are: V_{dd}=3.3V±10% and V_t=0.55 V±0.1. The area of allowed values for these limitations is shown in Figure 11, with a larger rectangle. For all values of V_{dd} and V_t inside this rectangle, system fulfills all given specifications. In A corner, system will have the highest delay, and in B corner the highest energy consumption. Constant speed and constant consumption lines are normalized at points A and B by normalization factors k_s and k_p, respectively. Based on that, we determine the influence

of position changes and the rectangle size in V_{dd}-V_t plane, onto consumption and system speed. For example, smaller rectangle on Figure 11 is defined with constraints V_{dd}=2.1 V±5% and V_t=0.18 V±0.05, and consumption is 60% (k_p=0.4) lower for the same operating speed (k_s=1).

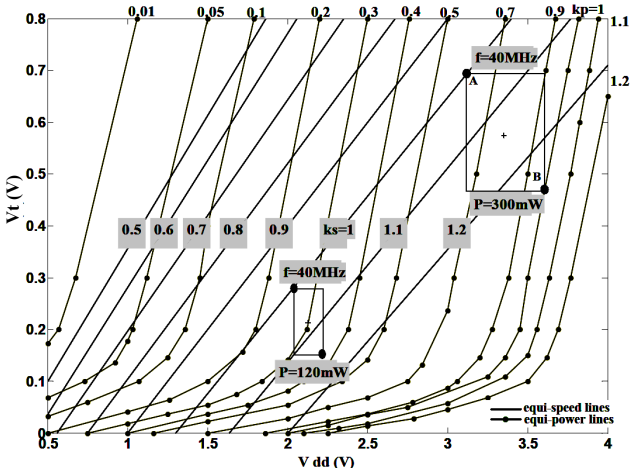

Fig. 11. V_{dd}-V_t plain with constant power consumption and delay lines

From all possible V_{dd}-V_t combinations that meet given time constraints, only one combination (V_{ddopt}, V_{topt}) guarantees minimal consumption. Shuster et. al. [18] proposed an equation, based on the transistor alpha model, for the calculation of total system consumption with the optimal (V_{ddopt}, V_{topt}) pair. Nevertheless, it should be stated that the continual change of V_{ddopt} and V_{topt} is unpractical. Designers are mostly allowed to choose between several discrete (V_{ddopt}, V_{topt}) values. By applying the multi V_{dd} technique, dynamic consumption can be reduced from 10%, up to 50%, whereas by applying the multi V_t technique, static consumption can be reduced for 50%, even up to 80% [3]. In [16], the optimal ratio between V_{dd} and V_t is given (Table III).

TABLE III. OPTIMAL RATIO OF V_{DD} AND V_T CONSIDERING CONSUMPTION

V_{ddi}, i=1,2,3,4, V_t=const	
(V_{dd1},V_{dd2}):	$\frac{V_{dd2}}{V_{dd1}} = 0.5 + 0.5\frac{V_t}{V_{dd1}}$
(V_{dd1},V_{dd2}, V_{dd3}):	$\frac{V_{dd2}}{V_{dd1}} = \frac{V_{dd3}}{V_{dd2}} = 0.6 + 0.4\frac{V_t}{V_{dd1}}$
(V_{dd1},V_{dd2}, V_{dd3}, V_{dd4}):	$\frac{V_{dd2}}{V_{dd1}} = \frac{V_{dd3}}{V_{dd2}} = \frac{V_{dd4}}{V_{dd3}} = 0.7 + 0.3\frac{V_t}{V_{dd1}}$
V_{ti}, i=1,2,3,4, V_{dd}=const	
(V_{t1},V_{t2}):	$V_{t2}=0.1V_{dd}+V_{t1}$
(V_{t1},V_{t2}, V_{t3}):	$V_{t2}=0.06V_{dd}+V_{t1}$ $V_{t3}=0.07V_{dd}+V_{t2}$
(V_{t1},V_{t2}, V_{t3}, V_{t4}):	$V_{t2}=0.04V_{dd}+V_{t1}$ $V_{t3}=0.05V_{dd}+V_{t2}$ $V_{t4}=0.06V_{dd}+V_{t3}$

VI. CMOS LOW POWER TOPOLOGIES

Standard CMOS combinational logic demands a CMOS transistor pair per every input. However, various alternative topologies with the lower number of transistors have been developed. Besides, the increase of scale of function integration in VLSI integrated circuit, has led to a reduce of consumption or increase of speed at the same consumption level.

Among the first alternative CMOS digital logics is the transmission-gate logic. Unlike standard logic where the basic cell is the inverter, in transmission-gate logic, the basic cell is the transmission gate. While in standard logic circuits, output signals are separated from the inputs, here the input signal is transferred to the output via the transfer gate. Figure 12 shows a 2/1 multiplexer (2/1 MUX) in transmission-gate logic. Since the complementary signals are needed for transmission gate control, inverters are integral part of the network as well. The 2/1 MUX in Figure 12 consists of only three CMOS transistor pairs, while standard logic needs seven pairs.

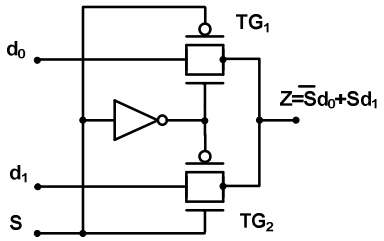

Fig. 12. MUX 2/1 in transmission-gate logic

Transmission gate logic can be additionally simplified by applying signals b and $\bar{b}$ to the inverter power line as in the example of XOR and XNOR circuit synthesis shown in Figure 13. The inverters with the (M_n, M_p) transistor pair are powered by b and $\bar{b}$ signals.

In the synthesis of logical functions in transmission-gate logic, it must be taken into account that between the output and at least one input, a contour of small resistance exists. Otherwise, output would be in the state of high impedance with the undefined logic level.

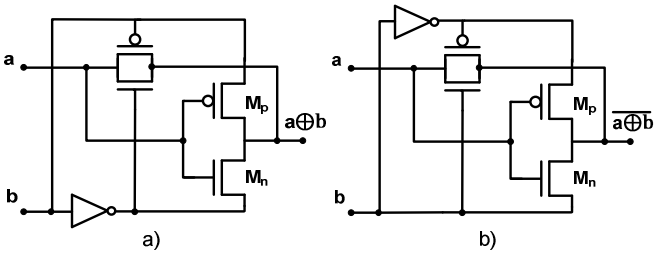

Fig. 13. (a) XOR and (b) XNOR circuits

As a transmission gate, instead of a CMOS pair, only nMOS transistors can be used (Fig. 14). The number of transistors is halved and the static consumption and the parasite

capacitance are reduced as well, which significantly increases the scale of function integration in a VLSI circuit.

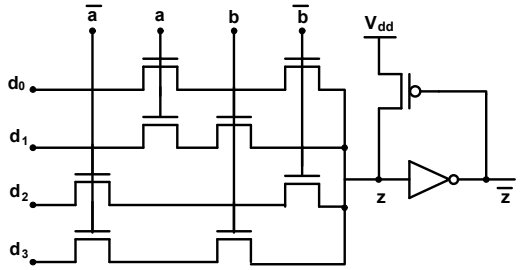

Fig. 14. MUX 4/1 in pass-transistor nMOS logic with true and complementary output

The problem with the nMOS pass-transistor logic is that the maximal voltage variation on one nMOS transistor is V_{dd}-V_{tn} and lower, for threshold voltage V_{tn} comparing to the CMOS transmission gate. That limits the number of serial transistors. Therefore, nMOS transistors with very low (NTL-*Non Threshold Logic*) or zero threshold voltage (ZTT-*Zero Threshold Logic*) have been used. The problem of mentioned logics lies in the low noise immunity.

Reduction of logic amplitude in nMOS transmission-gate logic is especially a problem when nMOS network ends with an inverter. That problem can be solved using a pMOS transistor M_p as shown in Figure 16. When $\overline{z}$ = 0, M_p is on and maintains the value of nMOS network output voltage at V_{dd}.

Low threshold transistors are used in the so-called CPL (*Complementary Pass-Transistor Logic*). This logic consists of two nMOS transistor networks with common control and complementary transfer signals (Figure 15).

PPL (*Push-pull Pass-transistor Logic*) [19] also have two transistor networks: one nMOS and the other pMOS (Figure 16). The control signals are common, and inputs are complementary. Output logic levels have been restored to V_{dd} and 0 by transistors M_p and M_n, respectively.

Table IV shows full adder comparative characteristics using different logics, implemented in 0.8 μm technology at V_{dd}=3.3 V. Although pMOS transistors are slower than nMOS, logic delay of PPL is approximately like CPL, but the consumption is significantly lower.

TABLE IV. FULL ADDER COMPARATIVE CHARACTERISTICS

Parameter	CMOS	CPL	PPL
Logic delay [ns]	1.57	0.84	0.83
Cons. [mW/100Hz]	1.90	1.33	0.42
$P{\cdot}t_d$ (normalized)	1	0.38	0.12

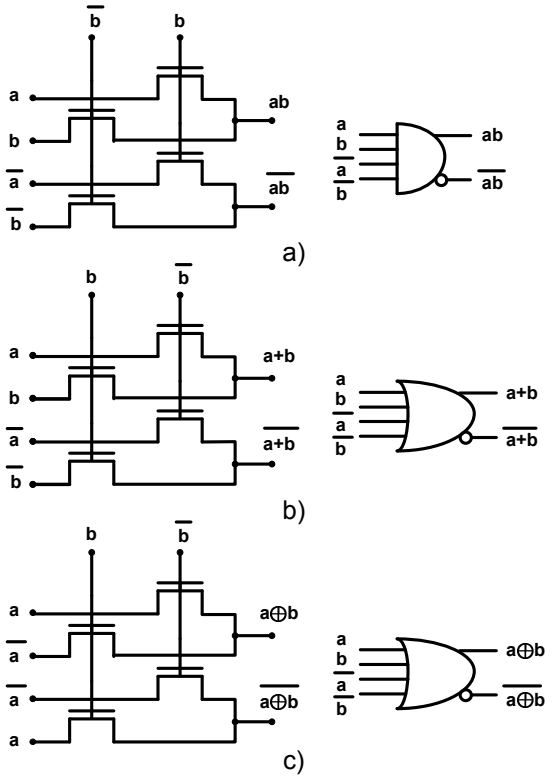

Fig. 15. AND/NAND (a), OR/NOR (b) i XOR/XNOR (c) logic circuits in CPL

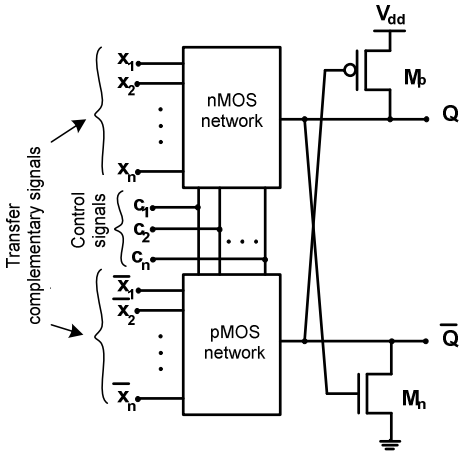

Fig. 16. PPL block sheme

VII. ADIABATIC LOGIC

The Term "adiabatic" describes thermodynamic processes in which the amount of heat remains constant (there is no exchange of energy with the environment). Adiabatic logic in the ideal sense, designate digital circuits without loss (dissipation) of electrical energy. In practice, it denotes the logic with minimal consumption of electrical energy during the switching of states. Adiabatic switching state shifting is a charge/discharge mechanism which returns accumulated

energy to the source inside the load capacitor using the dynamic power supply. Dynamic power supply or clocked power has a very important role in adiabatic logic, because beside power supply, it provides energy recovery.

Nowadays, there are many techniques of adiabatic logic [20-25]. Energy recovery process will be explained on the example of ECRL (*Efficient Charge Recovery Logic*) inverter (Figure 17). Power supply *PC* is with trapezoidal pulses.

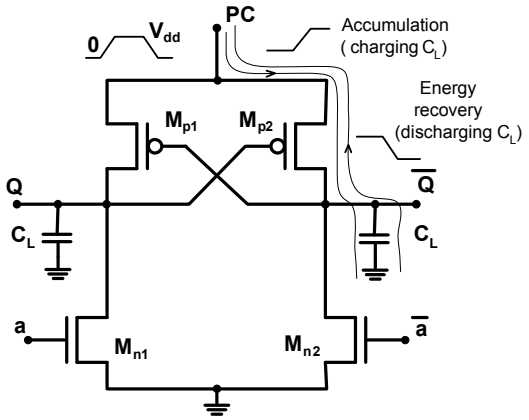

Fig. 17. ECRL inverter scheme

In the initial state holds a=1, and the M_{n1} is conducting (Q=0). While *PC* rises from 0 to V_{dd}, over conductive transistor M_{p2} the output $\overline{Q}$ follows the variation of *PC*. When *PC* reaches the V_{dd} value, then it holds $\overline{Q}$=1, and Q=0 and those conditions are valid logic states at inputs of next stage. During the fall of *PC* from V_{dd} to zero, the right capacitor C_L discharges over the conductive M_{p2} and *PC*, and therefore recovers accumulated energy to the *PC* supply.

More complex ECRL circuits have two complementary nMOS transistor networks with complementary excitations (Figure 18), instead of M_{n1} and M_{n2} transistors. Complementary networks are obtained by complementing input signals and switching of logic operators as a function of f_n nMOS network.

For example, f_n 2/1 multiplexer function is $f_n = (\overline{s}a + sb)$ and the function of complementary network is $\overline{f_n} = (s + \overline{a})(\overline{s} + \overline{a})$ (Figure 18b).

Other adiabatic topologies should be mentioned as well: PAL (*Pass-transistor Adiabatic Logic*) [21], CPAL (*Complementary* PAL), PFAL (*Positive Feedback Adiabatic Logic*) [20] etc. Reduced energy consumption comparing to standard CMOS logic is around 50 to 90%.

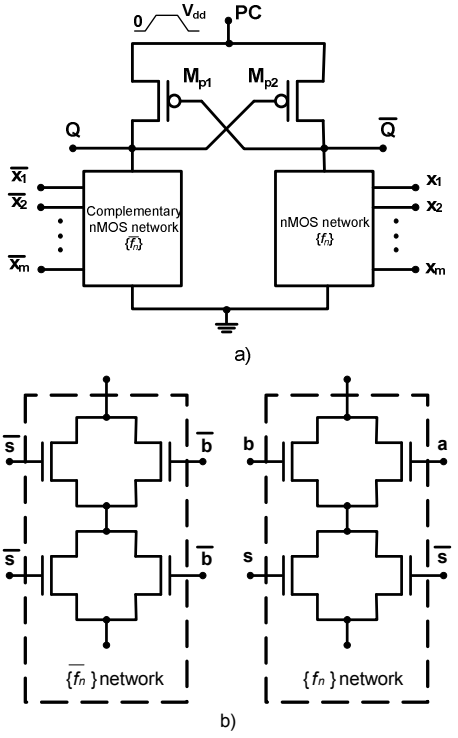

Fig. 18. (a) Block scheme of complex ECRL circuit (b) with f_n and $\overline{f_n}$ MUX2/1 network

VIII. CONCLUSION

To enable the design of energy-efficient digital systems, designers must take into account the electrical energy consumption through all design phases, from functional description to transistor level. The biggest energy saving (10 to 20 times) with the least time needed for consumption analysis is acquired on the system design level. In the sub-threshold regime, consumption is several orders of magnitude lower, but operating speed is lowered by nearly the same amount in comparison to the strong inversion regime. Rescaling of transistor dimensions increases gate current I_g which is very dependent on power supply. Multi V_t /V_{dd} design techniques provide the reduction of consumption to a scale of about ten percent at the same operating speed. Digital systems with two power supplies and/or two threshold voltages are optimal as well. Using two threshold voltages, static consumption can be reduced up to 80%. Alternative topologies provide larger scale of function integration per single VLSI circuit, lower consumption level and higher-speed rate. The transfer logic has the widest application in VLSI digital circuit design whereas adiabatic logic ensures the greatest energy saving (up to 90%).

REFERENCES

[1] R. Sarpeshkar, "Universal principles for ultra low power and energy efficient design", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 59, No.4, pp. 193-198, 2012

[2] J. Rabaey, Low power design essentials, Springer-Verlag, New York, 2009

[3] B. Jovanovic, Analytic model for dynamic consumption evaluation of arithmetic circuits implemented on FPGA, PhD thesis, Elektronski fakultet Niš, 2013

[4] S. R. Nassif, "Waiting for the Post-CMOS Godot", Int. ACM Great Lakes Symposium on VLSI, Lausanne, Switzerland, 2011

[5] K. Itoh, "A Historical Review of low-power, low-voltage digital MOS circuits development", IEEE Solid-State Circuits Magazine, Vol. 5, No. 1, pp 27-39, 2013

[6] T. Makimoto, "The Age of the Digital Nomad: Impact of CMOS innovation", IEEE Solid-State Circuits Magazine, Vol. 5, No. 1,pp 40-47, 2013

[7] Y. Tsividis, C. McAndrew, Operating and modeling o the MOS transistor, Oxford University Press, 2011

[8] B. Dokic, A. Pajkanovic, "Subthreshold operated CMOS analytic model", INDEL 2012, IX Symposium on Industrial Electronics, Banja Luka, Bosnia and Herzegovina, 2012

[9] A. Wang, B. H. Calhoun, A. P. Chandrakasan, Sub-threshold design for ultra low-power systems, Springer, 2006

[10] L. Nazhandali, B. Zhai, J. Olson, A. Reeves, M. Minuth, R. Helfand, S. Pant, T. Austin, D. Blaauw, "Energy optimization of subthreshold-voltage sensor network processes", ISCA'05, Proc. of the 32nd Int. Symp. on Computer Architecture, Madison, Wisconsin USA, 2005

[11] A. Mishra, R. A. Mishra, "Leakage current minimization in dynamic circuits using sleep switch", SCES 2012, Students Conference on Engineering and Systems, pp. 1-6, Allahabad, Uttar Pradesh, India, 2012

[12] B. L. Dokic, "Integrated circuits–digital and analog", Glas Srpski, 1999

[13] P. M. Petkovic, "Design of CMOS integrated circuits with mixed signals", Elektronski fakultet Niš, 2009

[14] M. Amis, S. Areibi, M. Elmasry, "Design and optimisation of multithreshold CMOS (MTCMOS) circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No 10, pp. 1324 – 1342, 2003

[15] S. Shigematsu, S. Mutoh, Y. Matsuya, Y. Tanabe, J. Yamada, "A 1-V High-Speed MTCMOS Circuit Scheme for Power-Down Application Circuits", IEEE Journal of Solid-State Circuits, Vol. 32 No. 6, pp. 861–869, 1997

[16] M. Hamada, Y. Ootaguro, T. Kuroda, "Utilizing surplus supplies timing for power reduction", IEEE Conference on Custom Integrated Circuits, pp. 89-92, San Diego, USA, 2001

[17] C. Piguet, C. Schuster, J. Nagel "Static and Dynamic Power Reduction by Architecture Selection", Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation. Lecture Notes in Computer Science, Vol. 4148, pp. 659-668, 2006

[18] C. Schuster, J. L. Nagel, C. Piguet, P. A. Farine, "Architectural and Technology Influence on the Optimal Total Power Consumption", Proceedings of Design, Automation and Test in Europe (DATE '06), pp 13-19, Munich, 2006

[19] W. H. Paik, H. J. Ki, S. W. Kim "Low power logic design using push-pull pass-transistor logics", International Journal of Electronics, Vol. 84, No. 5, pp. 467-478, 1998

[20] R. K. Yadav, A. K. Rana, S. Chauhan, D. Ranka, K. Yadav, "Adiabatic technique for energy efficient logic circuits design", International Conference on Emerging Trends in Electrical and Computer Technology (ICETECT 2011), pp 776-780, Tamil Nadu, 2011

[21] V. G. Oklobdzija, D. Maksimovic, L. Fengcheng, "Pass-transistor adiabatic logic using single power-clock supply", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 44, No. 10, pp. 842-846, 1997.

[22] A. K. Maurya, G. Kumar, "Energy efficient adiabatic logic for low power VLSI applications", International Conference on Communication Systems and Network Technologies (CSNT 2011), pp. 460-463, Katra, Jammu, 2011

[23] J. Hu, Q. Chen, "Modelling and near-threshold computing of power-gating adiabatic logic circuits", Przegląd Elektrotechniczny (Electrical Review), Vol. 88, No. 76, pp. 277-280, 2012

[24] D. Markovic, C. C. Wang, L. P. Alarcon, L. Tsung-Te, J. M. Rabaey, "Ultralow-power design in wear-threshold region", Proceedings of the IEEE , Vol. 98, No. 2, pp. 237-252, 2010

[25] A. Pajkanovic, T. J. Kazmierski, B. L. Dokic: Adiabatic Digital Circuits Based on Sub-threshold Operation of Pass-transistor and Slowly Ramping Signals, Proceedings of Small Systems Simulation Symposium, pp 48-53, Niš, 2012