# A Simple Square Rooting Circuit Based on Operational Amplifiers (OPAMPs)

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***Abstract*** **— A simple circuit which accepts a negative voltage as input and provides an output voltage equal to the square root of the input voltage is described in this paper. The square rooting operation is dependent only on the ratio of two resistors and a DC voltage. Hence, the required accuracy can be obtained by employing precision resistors and a stable reference voltage. The feasibility of the circuit is examined by testing the results on a proto type.**

***Keywords-square-rooting; generators; comparators; switches; low pass filters***

## I. INTRODUCTION

A need for obtaining the square root of a measured quantity is often met in the field of measurement and instrumentation systems [1]. Especially techniques that involve the measurement of unknown signals buried in excessive noise by employing either a Phase Sensitive Detector (PSD) or a tracking amplifier invariably need a final square rooting stage [2]. A square rooting circuit is also required in certain methods of determining impedances under sinusoidal excitation as well as in case of obtaining the three vectors of a 3 phase power system.

Methods based on expensive and complex multipliers have been proposed in the past for realizing a circuit that provides an output voltage whose magnitude is the square root of the input voltage. Square rooting circuits have been implemented with the use of different high performance active building blocks with second generation current conveyors [3], OTAs [4], second generation current controlled current conveyors (CCCIIs) [5], current differencing transconductance amplifiers (CDTAs) [6] and current follower transconductance amplifiers (CFTAs) [7].

Unfortunately, these reported circuits suffer from one or more of following disadvantages: (a) excessive use of the active/passive elements, especially external resistors [3-5], (b) use of a floating resistor, which is not convenient to further fabricate in IC [3] and (c) absence of linearly electronic controllability of output signal [3-7].

In this paper, a novel simple circuit for square rooting employing operational amplifiers (OPAMPs) which eliminates all drawbacks of the previously mentioned methods [3-7], is proposed. Though the scheme is simple, the expression for the output indicates that with a precision DC voltage as a reference and a pair of precision resistors, good accuracy can be achieved.

## II. CIRCUIT DESCRIPTION

The circuit diagram of the proposed scheme is shown in Figure 1. The sawtooth wave is generated by charging a capacitor at a specified rate and then rapidly discharging it with a switch. Let us assume that at start, the charge and, hence, the voltage at the output terminal of operational amplifier $OA_1$ is zero. Since the inverting terminal of the operational amplifier $OA_1$ is at virtual ground, the current through $R_1$, namely $V_R/R_1$ Amps, would flow through and charge capacitor $C_1$. During this charging (till the output of $OA_1$ reaches the voltage level of $V_R$) the output of the operational amplifier $OA_2$, configured to work as a comparator, is at the LOW state and switch $S_1$ is kept open (OFF). As soon as the output of $OA_1$ crosses the level of $V_R$, e.g. after a time period $T$, the output of comparator $OA_2$ goes high and switch $S_1$ is closed (ON). The $S_1$ switch would then short the capacitor $C_1$ and hence $V_S$ drops to zero volts. During the time period $T$ we have,

$$V_S = \frac{1}{R_1C_1}\int V_R dt = \frac{V_R}{R_1C_1}t \qquad (1)$$

After a very short delay time $Td$, required for the capacitor to discharge to zero volts, the comparator $OA_2$ output returns to LOW and switch $S_1$ is opened, thus allowing $C_1$ to resume charging. This cycle, therefore, repeats itself at a period $(T+Td)$. The waveforms at cardinal points in the circuit of Figure 1 are shown in Figure 2. From (1) and the fact that at time $t=T$, $V_S=V_R$, we get:

$$T = R_1C_1 \qquad (2)$$

As seen in Figure 1, the comparator $OA_3$ compares the sawtooth waveform thus generated with the output voltage $V_O$

and provides at its output, a pulse train $V_K$. The ON time of this pulse train will be:

$$D = \frac{V_O}{V_R} T \qquad (3)$$

This pulse train $V_K$ controls switch *S2*. Switch *S2* connects (a) *Vo* to the low pass filter realized with the operational amplifier OA4 during ON time 'D' and (b) zero volts during OFF time of pulse train $V_K$. Another pulse train $V_P$ is generated at the output of switch *S2* with the same ON time 'D', period *T* and max value *Vo*. The output of the low pass filter realized with the operational amplifier OA4 will be the average value of pulse $V_P$ which is,

$$V_F = \frac{1}{T}\int_0^D V_O dt = \frac{V_O}{T} D = \frac{V_O^2}{V_R} \qquad (4)$$

Considering KCL for node 'J' in the circuit of Figure 1, we get:

$$I_1 + I_3 = I_2$$

$$I_1 = \frac{V_F}{R_3}$$

$$\frac{V_O^2}{R_3 V_R} + \frac{V_O}{R_5} = \frac{V_I}{R_4}$$

If $R_3 = R_4 = R$ and $R_5 >> R$

$$\frac{V_O^2}{V_R} = V_I$$

$$V_O^2 = V_I V_R$$

$$V_O = \sqrt{V_I V_R} \qquad (5)$$

Thus the output voltage $V_O$ is proportional to the square root of the input voltage $V_I$.

## III. EXPERIMENTAL RESULTS AND CONCLUSION

The circuit shown in Figure 1 was implemented and tested in our Laboratory. LF 356 ICs were used for all operational amplifiers. Switches $S_1$ and $S_2$ were realized with CD 4053. The following values were set for different circuit components; $V_R$=6 V, $R_1$=200 kΩ, $C_1$=470 pF, $R_3$=$R_4$=10 kΩ, $R_5$=1 MΩ. Voltage levels of ±7.5 V were chosen for the power supply. The test results are shown in Table I.

The accuracy of the proposed circuit strongly depends upon the sharpness and linearity of the sawtooth waveform. The offset voltages of all operational amplifiers are to be nulled for better performance of the circuit. The small variations in voltage $V_R$ will cause an error at the output; hence, a stable precision voltage source must be used as $V_R$. However the small variations in the power supply will not affect the circuit at all. It should be noted here that the polarity of input voltage $V_I$ should only be negative and its maximum value should be less than $V_R$. Experimental results indicate the practical feasibility of the proposed circuit.

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TABLE I. TEST RESULTS ON THE PROTO TYPE SQUARE ROOTING CIRCUIT

| Input Volts $-V_I$ | Output Voltage by Experiment | Output Voltage by Calculation | Error in % |
|---|---|---|---|
| 0.5V | 1.711 | 1.732 | -1.20 |
| 1.0V | 2.420 | 2.449 | -1.18 |
| 1.5V | 2.959 | 3.000 | -1.34 |
| 2.0V | 3.414 | 3.464 | -1.44 |
| 2.5V | 3.829 | 3.872 | -1.10 |
| 3.0V | 4.200 | 4.242 | -0.99 |
| 3.5V | 4.525 | 4.582 | -1.24 |
| 4.0V | 4.820 | 4.890 | -1.43 |
| 4.5V | 5.125 | 5.196 | -1.35 |

## REFERENCES

[1] E. O. Doebelin, Measurement systems: application and design, Mc Graw Hill, New York, 2004

[2] M. A. Atmanand, "Novel Schemes for impedance measurement and their implementation through electronic circuits", Ph.D Thesis, IIT Madras, 1996

[3] S. I. Liu, "Square-rooting and vector summation circuits using current conveyors", IEE Proc. Circuits., Dev. Syst., Vol. 142, No. 4, pp. 223-226, 1995.

[4] V. Riewruja, "Simple square rooting circuit using OTAs", Electronics Letters, Vol. 44, No. 17, pp. 1000-1002, 2008

[5] C. Netbut, M. Kumngern, P. Prommee, K. Dejhan, "New simple square rooting circuits based on translinear current conveyors", ECTI Tranasactions on Elecrtrical Eng., Electronics and Communication, Vol. 5, No. 1, pp. 10-17, 2007.

[6] W. Tangsrirat, T. Pukkalanun, P. Mongkolwai, W. Surakampontorn, "Simple current mode analog multiplier, divider, square-rooter and square based on CDTAs", AEU-Int. J. Electron. Commun., Vol. 65, No. 3, pp. 198-203, 2011.

[7] P. Mongkolwai, D. Prasertsom, W. Tangsrirat, "CFTA- based current controlled current amplifier and its application", 25th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC 2010), Pattaya, Thailand, 2010.

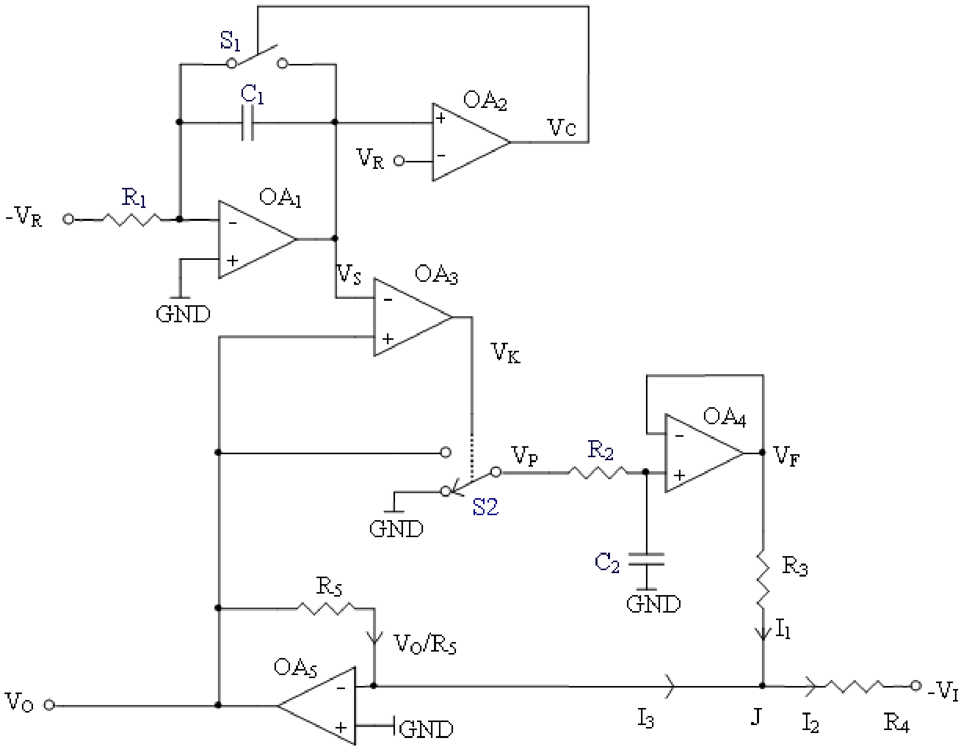


Fig. 1. Circuit diagram of square rooter

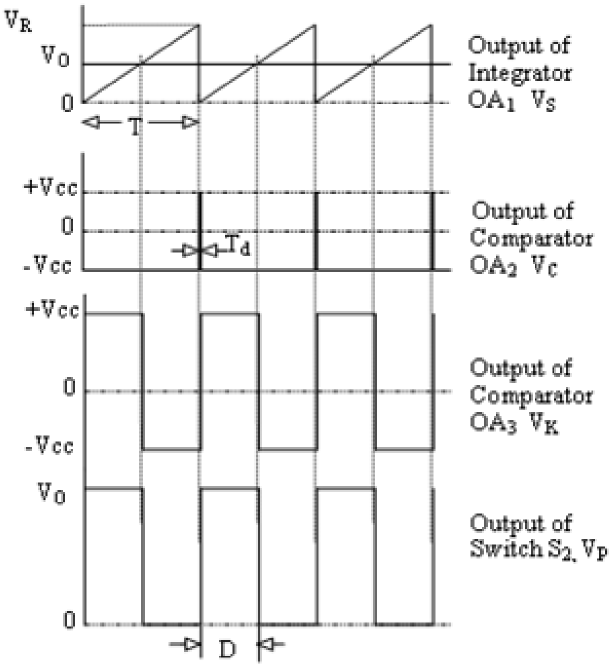


Fig. 2. Associated waveforms of Figure 1

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