CHEMICAL ENGINEERING TRANSACTIONS
VOL. 62, 2017
A publication of AIDIC
The Italian Association of Chemical Engineering
Online at www.aidic.it/cet
Guest Editors: Zhuo Yang, Junjie Ba, Jing Pan

ISBN 978-88-95608- 49-5; **ISSN** 2283-9216
DOI: 10.3303/CET1762194

Study on Hot Carriers Effect of Uniaxial Strained Si NMOS

Wang Ying

Shaanxi Xueqian Normal University, Xi'an 710100, China
wayag@163.com

The hot carrier effect of strained Si MOS is more significant than that of bulk Si MOS. Based on the study of the mechanism of hot carrier effect in uniaxial strained Si MOS, the factors affecting the hot carrier effect of uniaxial strain Si MOS and the effect on the electrical characteristics of the device are analyzed. The models of hot carrier collision ionization rate, interface state and threshold voltage degradation of uniaxial strain Si NMOS devices are established. The simulation results show that the threshold voltage shift is proportional to the interface state. When the interface state reached 1E8, the threshold voltage began to drift significantly. And reaching 1E12, the interface state reached saturation. With the increase of stress time, the shift of threshold voltage is decreasing.

1. Introduction

Strain Si material has high carrier sub mobility, and it is compatible with the traditional Si technique, which is a research hot-spot at home and abroad. What's more, because of the decrease of band gap of Si strain and the increase of carrier mobility and other factors, the hot carrier effect of Si strain MOS is more significant. The degradation of MOS devices due to hot carrier effect is mainly due to the interface states and oxide sink charges produced by the "hot electrons" and "hot holes" injection into the Si/SiO_2 interface and the SiO_2 layer. With the increase of interface charge, the parameters of the device changed. When the interfacial charge is accumulated to a certain extent, the device performance may be invalid. Therefore, the reliability of strained Si MOS devices has become a bottleneck restricting its development.

2. Formation mechanism of hot carrier effect in uniaxial strain Si NMOS

The structure of SiN stress cap layer / polysilicon gate / gate oxygen / strain Si channel / substrate is used from top to bottom. The thickness of the nitrogen oxide layer is 75Nm, which is the stress source of the device (Al-Ameri et al., 2017); the thickness of the Poly-Si is 150nm; the thickness of the gate oxide layer is 2nm; and the substrate is P type (100) crystal to the Si single crystal; the source drain injection dose is $3.5\times10^{15}cm^{-3}$.

Hot carrier effect is a physical mechanism under the electric stress of MOSFET. In the uniaxial strain Si MOS, due to the narrowing of the band gap and the increase of carrier mobility, the hot carrier effect leads to the degradation of the device performance far more than the relaxation Si MOS. In addition, the deposition of stress cap layers of the uniaxial strain Si NMOS may also cause increasing degradation. This is because in the chemical vapor deposition (CVD) SiN, compounds such as SiH_4 and NH_3 containing H are used, and a large number of H will be included inside. The generation of interface traps (N_{it}) from the hot carrier effect causes the drift of the device threshold voltage and the decrease of the driving current (I_d) and the trans-conductance (g_m) (Kumar et al., 2016). The performance changes of these devices will affect the performance of the whole circuit.

Firstly, it is assumed that the interface state is the main reason for the degradation of the device, and the trapped charge of the oxide layer is the secondary cause, while the interface state is located near the drain, so the density and mobility of the carrier can only be reduced locally.

Secondly, because the barrier of oxide layer is about 3.2eV, and breaking the Si-H bond and Si-OH respectively requires 0.3eV and 0.35eV, it is known that the interface state is produced by the hot electrons with 3.5eV or more energy (Kumar et al., 2016).

Please cite this article as: Wang Ying, 2017, Study on hot carriers effect of uniaxial strained si nmos, Chemical Engineering Transactions, 62, 1159-1164 DOI:10.3303/CET1762194

Thirdly, if the Si-H key interrupts hot electron generation, dangling bonds Si· and hydrogen ion are compound, there would be no interface states and it had no effect on the device. But if H_i diffuses and gets away from the interface, the existence of dangling bond Si· will lead to the emergence of the interface states. The reaction equation is:

$$\equiv Si-H \rightarrow Si\cdot + H_i \tag{1}$$

The rate of hot carrier interruption of the Si-H bond can be expressed as:

$$K \cdot J_{BB} \tag{2}$$

n the above formula, K is the breaking rate parameter, which is directly proportional to the density of Si-H at the interface; J_{BB} is the breaking bond current. Assuming that the recombination rate between dangling bond Si· and hydrogen ion Hi is:

$$\beta_p N_{it} n_H(0) \tag{3}$$

In the above formula, N_{it} is the interface state density, nH is the hydrogen ion Hi density at the interface, and the β_p is constant. The net generation rate of interface states can be obtained by combining the above two equations:

$$\frac{dN_{it}}{dt} = KJ_{BB} - \beta_p N_{it} n_H(0) \tag{4}$$

Considering the rate of interface state generation, the rate of diffusion of hydrogen ion Hi from the interface is far from the interface, and it can be obtained from the diffusion equation:

$$\frac{dN_{it}}{dt} = D_H \frac{n_H(0)}{x_H} \tag{5}$$

DH and H_i are the diffusion coefficients, and xH is the diffusion length of H_i. The formula (5) can be obtained by substituting into (4).

$$\frac{dN_{it}}{dt}\left[1+\beta_p \frac{x_H}{D_H} N_{it}\right] = KJ_{BB} \tag{6}$$

Ideally, the initial interface state density is N_{it}=0, so:

$$N_{it} = \frac{D_H}{\beta_p x_H}\left(tJ_{BB}\frac{2K_e\beta_p x_H}{D_H}\right)^{1/2} \tag{7}$$

The acceptor and donor traps at any position are specified with the corresponding capture interface in the oxide and semiconductor interface (Richard et al., 2015). By computing a function of stress by performing transient degradation of device, trap rate equation is performed at each time step so that the capture electronic concentration is calculated. The captured electron trap can be described as the following equation.

$$\frac{dN_n(x,t)}{dt} = \frac{SIGMAE}{q}\cdot J_{inj,n}(x,t)\cdot\left(NTA(x)-N(x,t)\right) \tag{8}$$

$$\frac{dN(x,t)}{dt} = \frac{SIGMAH}{q}\cdot J_{inj,p}(x,t)\cdot\left(NTD(x)-N(x,t)\right) \tag{9}$$

Here N(x, t) represents the concentration of electrons trapped at the interface X point and time T in transient simulation, and NTA and NTD are the densities of acceptor and donor traps at the 0 moment. $J_{inj,\,n}$(x, t) and $J_{inj,\,P}$(x, t) are the injected electron and hole current densities, and SIGMAE and SIGMAH are the capture cross sections of electrons and holes. In this simulation study, NTA and NTD control the total amount of degradation,

while SIGMAE and SIGMAH control the degradation speed of the device in the degradation process, and the larger the value, the greater the degradation in unit time.

3. Impact ionization rate model

Under the action of large electric field, the formation rate of hole electron pairs produced by collision ionization is:

$$G_{impact} = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q} \tag{10}$$

Ionization rates of electrons and hole, α_n and α_p, are defined as the number of electron hole pairs produced by carrier unit distance transmission.

$$\alpha_n = \frac{1}{nV_n} \int_{BS1}^{BS2} f\left(x,k,t\right) R_{ii,n} d^3k \tag{11}$$

The above integral formula is applicable to all the energy band structures in semiconductors, and it can be seen from the upper formula that the impact ionization rate is a function of energy. Based on the drift diffusion model, the use of the empirical formula, impact ionization rate can be calculated by the local electric field.

$$\alpha_n = a_n exp\left(-\frac{b_n}{E}\right) \tag{12}$$

The upper model is based on the assumption that the carrier is in a state of equilibrium in the local electric field. However, the injection of hot carriers will break this assumption, because carriers are in an unbalanced state in the lattice (Song et al., 2016). The average carrier temperature can be obtained by solving the energy balance equation, so the ionization rate can be converted to the model depending on the energy.

$$\alpha_{n,p}\left(T_{n,p}T_L\right) = A_i exp\left(-\frac{B_i}{E_{n,p}}\right) \tag{13}$$

A_i and B_i are semi empirical parameters obtained by experiment or MC simulation. Since the substrate in MOS devices is a direct result of the current ionization rate, generally, the ratio of substrate current to leakage current is used to represent the ionization rate. It can be seen from the above model that, due to the influence of hot carrier effect, A_i and B_i will be reduced, so the ionization rate will decrease.

4. Uniaxial strain Si MOS interface characteristics

The distribution function of acceptor interface traps is similar to the distribution function of impurity levels in semiconductors.

$$F_{SA}\left(E_t\right) = \left[\frac{1}{1+\left(1/g_A\right)\exp\left[\left(E_t - E_F\right)/k\mathrm{T}\right]}\right] \tag{14}$$

In the formula, E_t is the energy of the interface trap, and for the acceptor, the ground state degeneracy is 4. It is assumed that each interface has two interface states, and D_{it} can be used for equivalent interface state distribution (Subbaraman et al., 2015). It is assumed that the neutral energy level E_0 exists, and the state above this level is the acceptor, and the state below this level is the donor. Using the approximation of the carrier distribution in the semiconductor, the occupancy rate of EF higher than the Fermi level is 0, and the occupancy rate below EF is 1. According to the above approximation, the charge of the interface is:

$$Q_{\mathrm{it}} = -q\int_{E_0}^{E_F} D_{it}dE = +q\int_{E_F}^{E_0} D_{it}dE$$

Because the interface traps are distributed in the band gap, they are represented by the interface trap distribution:

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE}$$

5. Threshold voltage degeneration model

The empirical formula is found for the mobility μ and the density of interface states in the channel inversion layer:

$$\mu = \frac{\mu_0}{1 + KN_{it}(y)} \tag{15}$$

In the above formula, μ_0 refers to the inversion layer mobility with no degeneration and $N_{it}(y)=0$, and K is an empirical constant.
The average interface state density and the oxide trap charge are defined as:

$$N_{it} = \frac{1}{L_{eff}}\int_0^{L_{eff}} N_{it}(y)dy \tag{16}$$

$$N_{ox} = \frac{1}{L_{eff}}\int_0^{L_{eff}} N_{ox}(y)dy \tag{17}$$

In the above formula, l refers to the length of device damage zone. When Vds is quite small in the linear area, the second term can be approximated as $\frac{\mu_0 W_{\text{eff}}}{L_{\text{eff}}} q\left(\bar{N}_{\text{it}} + \bar{N}_{\text{ox}}\right)$.

The empirical formula of the inverse layer mobility and the interface state substituted into the upper form, and then we can obtain (Wirths et al., 2015):

$$\left(1 + \mathrm{K}\bar{N}_{\text{it}}\right) I_{\text{ds}} = \frac{\mu_0 W_{\text{eff}}}{L_{\text{eff}}} C_{\text{ox}}\left(V_g - V_T\right)V_{\text{ds}} - \frac{\mu_0 W_{\text{eff}} V_{\text{ds}}}{L} q\left(\bar{N}_{\text{it}} + \bar{N}_{\text{ox}}\right) \tag{18}$$

The above formula is transformed into:

$$V_{T1} = V_g - \frac{q\left(\bar{N}_{\text{it}} + \bar{N}_{\text{ox}}\right)}{C_{\text{ox}}} - \frac{I_d L_{\text{eff}}}{\mu_0 W_{\text{eff}} C_{\text{ox}} V_{\text{ds}}} - \frac{K\left(\bar{N}_{\text{it}} + \bar{N}_{\text{ox}}\right) I_{\text{ds}} L_{\text{eff}}}{\mu_0 W_{\text{eff}} C_{\text{ox}} V_{\text{ds}}} \tag{19}$$

$\Delta\bar{N}_{it}$ and $\Delta\bar{N}_{ox}$ are used to represent the increase of interface states and trapped charges in the oxide layer, and then it is obtained:

$$V_{T2} = V_g - \frac{q\left(\bar{N}_{\text{it}} + \bar{N}_{\text{ox}} + \Delta\bar{N}_{\text{it}} + \Delta\bar{N}_{\text{ox}}\right)}{C_{\text{ox}}} - \frac{I_d L_{\text{eff}}}{\mu_0 W_{\text{eff}} C_{\text{ox}} V_{\text{ds}}} - \frac{K\left(\bar{N}_{\text{it}} + \bar{N}_{\text{ox}} + \Delta\bar{N}_{\text{it}} + \Delta\bar{N}_{\text{ox}}\right) I_{\text{ds}} L_{\text{eff}}}{\mu_0 W_{\text{eff}} C_{\text{ox}} V_{\text{ds}}} \tag{20}$$

When $\Delta V_T = V_{T1} - V_{T2}$, we can get threshold voltage degradation:

$$\Delta V_T = \left(\frac{K I_{\text{ds}} L_{\text{eff}}}{\mu_0 W_{\text{eff}} C_{\text{ox}} V_{\text{ds}}} + \frac{q}{C_{\text{ox}}}\right)\left(\Delta\bar{N}_{\text{it}} + \Delta\bar{N}_{\text{ox}}\right) \tag{21}$$

The degradation of the device threshold voltage is directly proportional to the interface state and the amount of oxide trapped charge. Because of the threshold voltage $V_T = V_{FB} + var$ iables has no relation with time in MOS device, $\Delta V_T(t) = \Delta V_{FB}(t)$. As a result, hot carrier injection in VLSI is the main reason leading to the drift of threshold voltage with time.

6. Results simulation and analysis

Transient simulation is done for uniaxial Si NMOS device under high voltage of Vg=1.2V and Vd=2.4V. Then, the degeneration relationship of impact ionization rate affected by thermal carrier effect with time is obtained.

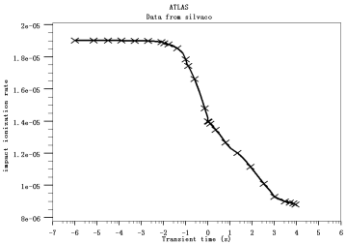

Figure 1: Degeneration of uniaxial Si NMOS impact ionization rate with time

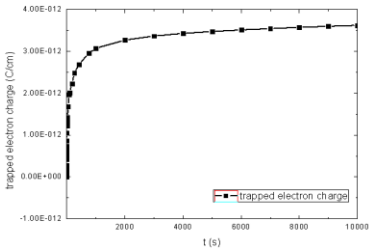

Figure 2: Increase of trapped electron charge with time in uniaxial Si NMOS

It is found from Figure 1 that the impact ionization rate of uniaxial strain Si NMOS decreases with the increase of time due to the effect of hot carrier effect. This is due to the decrease of the transverse electric field in the channel due to the generation of the interface state, resulting in a decrease in the impact ionization rate. This has the same trend as the model established previously.

It can be seen from Figure 2 that in the case of large voltage degradation, the trapping rate of trapped electron charge increases rapidly at the beginning, and after reaching a certain extent, the trapped electron charge begins to saturate (Zoellner et al., 2015).

It can be found from the figure 3 that the gate capacitance Cgg of the uniaxial strain Si NMOS device is larger than the gate capacitance of the relaxation Si NMOS device. This is because uniaxial stress causes the conduction band splitting and the effective mass change. These two factors affect the CV characteristic curve from different aspects. One is the simultaneous consideration of the band splitting and the effective mass change, and the other is that only the splitting of the energy band is considered. In uniaxial strain, the effect of energy band splitting on CV is not obvious, and the change of effective mass is the main reason for the change of CV curve. The uniaxial strain causes the change of the density of states and the quantum effective mass, and their change will directly affect the inversion layer charge, the reverse layer capacitance and the gate capacitance change. Therefore, the Cgg of uniaxial strain Si MOS is significantly larger than that of relaxation Si MOS.

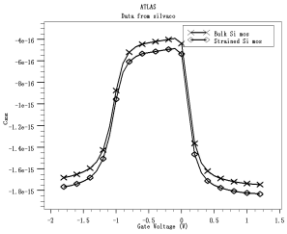

Figure 3: Uniaxial strain Si NMOS and relaxation Si NMOS gate capacitance

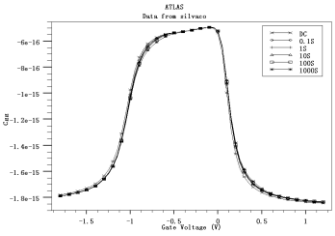

Figure 4: Degeneration of uniaxial strain Si NMOS gate capacitance with time

From Figure 4, it is found that the interface traps cause a significant extension of the CV curve along the voltage direction. This is due to the hot carrier effect, the total amount of interface state increases with the accumulation of time, which causes the drift of flat band capacitance with CV characteristics. With the saturation of interface states, the degradation of CV curve will become saturated. The simulation results are in agreement with the theoretical analysis.

The threshold voltage degradation model of the above uniaxial strain Si NMOS is simulated by Matlab, and the influence of interface state on threshold voltage is considered in the simulation. The simulation results are shown in figure 5.

It can be seen from figure 6 that the threshold voltage drift is directly proportional to the interface state. When the total amount of the interface state reaches 1 x 108, the threshold voltage begins to drift obviously, which is

consistent with the theoretical reports. When the interface state reaches 1 x 1012, the interface state reaches saturation, and the threshold voltage drift almost stops.

Figure 6 is the degradation relation of the threshold voltage with time for a uniaxial strain Si NMOS device degraded under high electrical stress conditions of Vg=1.2V and Vd=2.4V. DC scanning is performed at 0.01s, 0.1s, 1s, 10s, 100s, 1000s and 10000s time nodes, respectively.

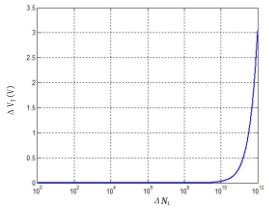

Figure 5: The relationship between the threshold voltage and interface state

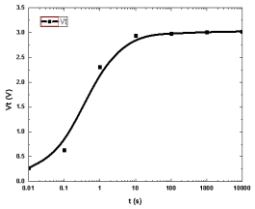

Figure 6: the degradation relation of the threshold voltage with time for a uniaxial strain Si NMOS device

7. Conclusion

This paper focuses on the generation mechanism of uniaxial strain Si MOS hot carrier effect. In addition, it establishes uniaxial strain Si NMOS device hot carrier impact ionization rate, interface state, threshold voltage degradation and so on models. Through analog simulation, it analyzes the influences of the device hot carrier effect on device performance, to provide theoretical and practical support for the development and application of uniaxial strain Si CMOS integrated circuit.

Reference

Al-Ameri T., Georgiev V, P., Adamu-Lema F., Asenov A., 2017, Simulation study of vertically stacked lateral si nanowires transistors for 5 nm cmos applications, IEEE Journal of the Electron Devices Society, (99), 1-1, DOI: 10.1109/jeds.2017.2752465

Kumar M., Kumar S., Goel E., Singh K., Singh B., Jit S., 2016, Strain-induced plasma radiation in terahertz domain in strained-si-on-insulator mosfets, IEEE Transactions on Plasma Science, 44(3), 245-249, DOI: 10.1109/tps.2016.2516588

Kumar S., Kumari A., Das M.K., 2016, Development of a simulator for analyzing some performance parameters of nanoscale strained silicon mosfet-based cmos inverters, Microelectronics Journal, 55, 8-18, DOI: 10.1016/j.mejo.2016.06.009

Richard M, A., Zoellner M.H., Chahine G.A., Zaumseil P., Capellini, G., Haeberlen, M., 2015, Structural mapping of functional ge layers grown on graded sige buffers for sub-10 nm cmos applications using advanced x-ray nano-diffraction, Acs Applied Materials & Interfaces, 7(48), 26696, DOI: 10.1021/acsami.5b08645

Song J.J., Zhu H., Zhang H.M., Hu H.Y., Xuan R.X., Shu, B., 2016, Hole mobility in arbitrary orientation/typical plane uniaxially-strained si materials, Silicon, 8(3), 381-389, DOI: 10.1007/s12633-015-9336-1

Subbaraman H., Xu X., Hosseini A., Zhang X., Zhang Y., Kwong D., 2015, Recent advances in silicon-based passive and active optical interconnects, Optics Express, 23(3), 2487-510, DOI: 10.1364/oe.23.002487

Wirths S., Troitsch R., Mussler G., Hartmann J., Zaumseil P., Schroeder T., 2015, Ternary and quaternary ni(si)ge(sn) contact formation for highly strained ge p- and n-mosfets, Semiconductor Science & Technology, 30(1), 055003, DOI: 10.1088/0268-1242/30/5/055003

Zoellner M, H., Richard M.I., Chahine G., Zaumseil P., Reich C., Capellini G., 2015, Imaging structure and composition homogeneity of 300 mm sige virtual substrates for advanced cmos applications by scanning x-ray diffraction microscopy, Acs Applied Materials & Interfaces, 7(17), 9031, DOI: 10.1021/am508968b