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Experimental, Modelling and Theoretical Study of CNT Growth and Connection on a Flip - Chip Device to Improve Thermal Management Performances

Maria Sarno, Rosangela Piscitelli*, Francesco Marra, Claudia Cirillo, Paolo Ciambelli

Department of Industrial Engineering and Centre NANO_MATES, University of Salerno
Via Giovanni Paolo II ,132 - 84084 Fisciano (SA), Italy
rpiscitelli@unisa.it

Here we report an experimental, modelling and theoretical study of CNT growth and connection on a chip device with a flip chip configuration used to improve thermal management performances, in order to elaborate board design analysis. CNTs growth was obtained for the first time on AlN substrate typically used in high power electronic. The thermal conductivity of isolated CNT was 1698,5 W/mK. Moreover, the aim of this paper was to study the role of the design parameters to mitigate the effects of a non-correct thermal management obtained with the help of high thermal conductive CNT connections bumps.
With the support of a simulator we evaluated thermal performances to help in a preliminary phase the board design. We worked on a configuration that would allow the direct integration into flip-chip devices in order to reduce the thermal contact resistance at interfaces from the die through the heat spreader and the junction temperature and thermal crosstalk.

1. Introduction

Constant improvements in power electronics has generated an unavoidable increase in power density, created more waste heat, reduced the efficiency and lowered the durability. This issues become even more challenging when coupled with compact size, light weight and lower cost requirements. Planning how to manage the waste heat in the preliminary phase of board layout design appears fundamental to mitigate the effects of a non-correct thermal management. High electron mobility transistors (HEMTs) with their high-power, high frequency and high temperature applications show a temperature increase, in channel region over 100°C than ambient temperature, as also confirmed by Wang et al. (Wang et al., 2013). Often, significant thermal contact resistance at multiple interfaces from the die through the heat spreader to the heat sink remains a challenging problem. Limited cooling capabilities give rise to localized heating spots, known as hotspots, at highly active regions of a chip as confirmed by Zhang et al. (Zhang et al., 2011). So, the possibility to have a connection medium which can itself improve heat dissipation between the substrate and the heat spreader appears the best solution: chip reliability improves and the thermal crosstalk through the channel region can be reduced.
Carbon nanotubes (CNTs) have been investigated as a thermal spreader medium to balance the temperature across the chip and reduce peak temperature. Indeed CNTs have excellent characteristics, such as high current handling capability and low resistance (Horibe et al, 2004), they also exhibit high thermal conductivity (Kim et al., 2001; Shioya et al., 2007), and high aspect structure (Soga et al., 2009).
Lu et al. (Lu et al., 2012) validated the possibility to use CNTs bumps in a flip-chip configuration to allow direct integration into devices, reducing the thermal contact resistance at interfaces and avoiding larger resistance due to defects via solders bumps. Indeed covalent bonds could improve adhesion and minimize thermal resistance, as stated by Kaur et al. (Kaur et al., 2014). The flip-chip connection has many advantages compared to the wire bonding connections in term of thermal and electrical aspects.

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Here we report an experimental, modelling and theoretical study of CNT growth and connection on a chip device with a flip chip configuration used to improve thermal management performances, in order to elaborate board design analysis. In particular, CNTs growth by a Chemical Vapour Deposition (CVD) for the first time on an AlN substrate, typically used for microelectronic applications, was obtained, and the thermal conductivity measured. The mechanism of CNT thermal management by COMSOL modelling was explored too.

2. Carbon nanotubes synthesis: experimental, results and discussion.

Carbon Nanotubes forests were prepared by CVD in a continuous flow microreactor. Before the synthesis, an optimized catalytic substrate, common deposition techniques resulted in CNTs forests peeling off, was obtained by deposition of nickel ferrites nanoparticles (NPs) (Altavilla et al., 2009) on aluminium nitride. Indeed, the "wet chemistry" approach used for the synthesis of the nanoparticles results in a nanohybrid of nickel ferrites NPs covered by hydrophobic organic chains improving wettability and adhesion on the AlN substrate.
Acetylene CVD, acetylene was chosen because permits thanks to its reactivity to growth CNT at lower temperature, was carried out in a continuous flow microreactor fed by acetylene–helium gas mixture. The temperature of catalyst bed was measured with a K thermocouple located inside a third coaxial quartz tube. The reactor was heated by an electrical oven, whose temperature is controlled by a temperature programmer–controller (Eurotherm 2408). Cylinder gases (99.998 pure acetylene and 99.9990 pure helium) were mixed to obtain the stream to feed the reactor. Constant flow rate of each gas was provided by mass flow controller. The reactor temperature was increased from 298K up to 873K under helium flow and then a 200 cm^3/min flow rate of 10% acetylene in helium was introduced in the reactor during 5 min. After this time, the feed flow was stopped and the reactor was cooled down to room temperature under helium flow.
The images in Figure 1 obtained with a scanning electron microscope (SEM) LEO 420 allow the observation of nanotubes inside the forest. Their outer diameters are in the range 20-50 nm (Figure 1b), their length reached few millimetres at increasing time (Figure 1c).

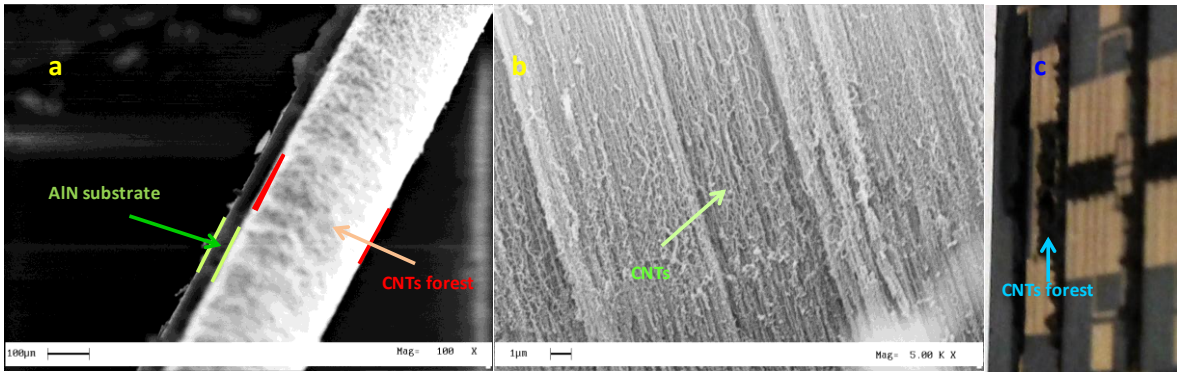

Figure 1: SEM image of AlN covered by a CNT forest (a, b). Photo of AlN covered by CNT forests, Au covers some areas of the devices.

In order to estimate our CNTs thermal conductivity we analyse Raman spectra finger print of an isolated CNT obtained at 873K for 5 min (Figure 2). G peak in the graphite based materials spectra manifest a strong temperature dependence and allows to monitor the local temperature change produced by the variation of the laser excitation power as stated by Balandin et al. (Balandin et al., 2008). Local temperature rise as a function of the laser power can be utilized to extract the value of the thermal conductivity. $K = 1/(2\pi h)(\Delta P/\Delta T)$, where h is CNT thickness and the local temperature rise ΔT is due to the changing heating power $\Delta P = P_2 - P_1$. Because the excitation power levels are relatively low, the G peak position linearly depends on the sample temperature $\omega = \omega_o + x_G T$. The final expression for the thermal conductivity in the radial heat wave case can be written as:

$$K = x_G \, 1/(2h\pi)(d\omega/dP)^{-1} \qquad (1)$$

where $d\omega$ is a small shift in the G peak position due to the variation dP in the heating power on the sample surface. We obtained a value of 1698,5 W/mK.

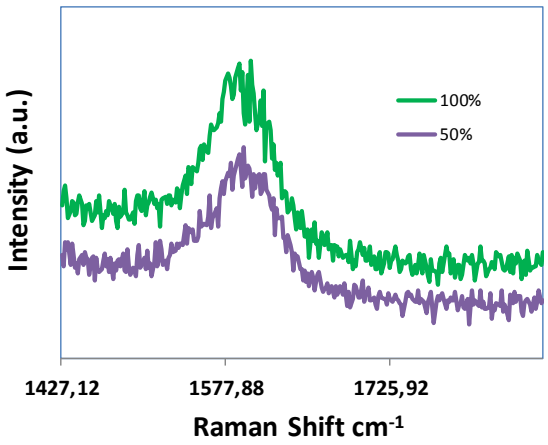

Figure 2: Raman spectra at two different laser power.

3. Numerical analysis

The numerical analysis of heat transfer in the flip-chip device has been conducted assuming the configuration and geometrical characteristics shown in Figure 3: chip layout (pHEMT FET in GaN / Sapphire technology); chip size: 1 mm x 0.8 mm x mm 0.33; gate area: 6 rectangular fingers (100 µm x 1 µm) at 50 µm distance; sapphire substrate thickness: 329 µm; FET mounted upside down, directly interconnected to the substrate through 6 bumps of carbon nanotubes: bumps dimensions are 100 x 40 µm and variable thickness: 10, 20, 30 microns; AlN substrate 1 cm x 1 cm x 0.6 mm.
As general approach, the following heat transfer equation has been considered in each subdomain:

$$\rho_i Cp_i \frac{\partial T_i}{\partial t} - \nabla \cdot (k_i \nabla T_i) = Q_i \qquad (2)$$

where the subscript i refers to the subdomain in which, time-by-time, the heat transfer equation is solved. At the boundary between two materials, continuity of temperature and heat flux has been considered. The heat source term Qi has been considered null everywhere except in the fingers.
The heat transfer equation (eq. 2) has been solved in fully 3D domain (constituted by subdomains representing the various materials involved in the flip-chip structure) and at stationary conditions, applying – as boundary conditions – a convective heat flux toward the air surrounding the flip-chip device, except for lower surface of AlN layer where a constant temperature of 313.15 K was imposed. Of course, each component has been characterized by its own thermal conductivity. In the case of fingers, a further term of heat source has been introduced, to take into account the 3 W of power generated by the fingers themselves. The set constituted by the heat transfer equation and boundary conditions equations has been compiled and solved by means of commercial package COMSOL 5.2, using a mesh discretization to solve from 46843 to 200000 degrees of freedom. The mathematical set has been solved in the fully 3D domain in order to reduce errors coming from 2D approximation in term of influence of gate width on self-heating end in terms of fingers number for the total thermal contribution (Bertoluzza et al., 2009). The three points in the figure below are used as temperature monitoring points. The positions were chosen basing on the criticality of spatial portion in order to maximize their thermal behaviour.

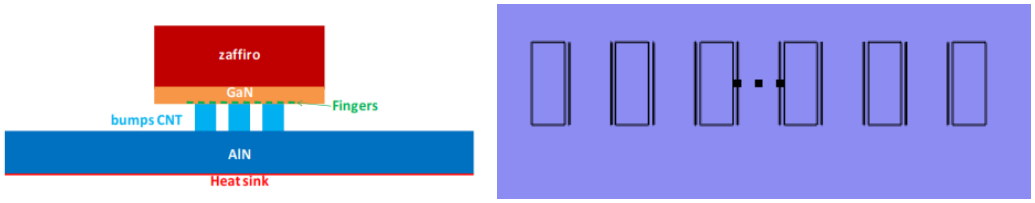

Figure 3: Sketch of flip-chip and planar view of the device.

The assumptions made for the simulations were: the device DC alimented; power dissipated by fingers: 3 Watt; the heat sink was simulated by the use of a wall at constant temperature of 40°C; CNT thermal conductivity was varied in the range: 60-3000 W/(m K). Chip was installed in the centre of the package. The scope of the simulations was to verify the cooling capacity of the heat spreaders in different configurations by monitoring chip temperature. Heat transfers through the mounted package to the surroundings for conduction and heat dissipates from all air-exposed surfaces for natural heat convection, which is modelled according to Newton law. The considered heat transfer model, based on Fourier law for heat conduiction, can efficiently and accurately describe the thermal effects at feature length scales much longer than the mean free path of phonons (i.e., 200-300 nm in silicon) as also investigated by Zhang et al. (Zhang et al., 2011).
In the nano-meter regime, where the mean free path of phonons approaches device feature scale, ballistic phonon transport is the primary heat transfer mechanism. Since the Fourier model cannot model this phenomenon accurately, other techniques such as the Gray phonon Boltzmann transport equation (BTE) under the relaxation time approximation can be used to model the nanometer device regions. On the other hand, our dimensions are larger than mean free path of phonons so the Fourier model can accurately describe our device's thermal properties.
In order to evaluate nanotubes thermal influence, we conducted four simulations set by varying the followings parameters:

- CNT's connection height,
- CNT's thermal conductivity;
- CNT number and spatial position
- device's thermal conditions.

CNT height significantly influences the capacity of heat dissipation in the various points of the channel region. Results show that the bumps of smaller thickness (10 μm) facilitate the dispersion of heat towards the substrate of aluminium nitride. Figure 4 reports the temperature results of the three configurations (20, 30, 40 microns' bumps) along x coordinate. The figure shows the simulations conducted using a k value of 60 W/(m K). No substantial differences in term of thermal crosstalk between the different configurations are found. The lowest temperature was recorded, as expected considering the increased conduction path, in the case in which the height of the connecting bumps is the smallest. This effect is more evident for low values of thermal conductivity (about 60 W/m K).
Increasing thermal conductivity, thermal management is improved, all the monitoring points show a smaller temperature value but this effect is mitigated after a given value of k: the temperatures reach practically constant values at a thermal conductivity of 1200 W/(m K), see Figure 4 that shows the temperature of monitoring centre point. Moreover, our simulations show that after this value, bumps thickness has no influence on the monitor points temperature. It can be seen from the figures that CNTs let the temperature decrease of about 30 °C in few microns length.

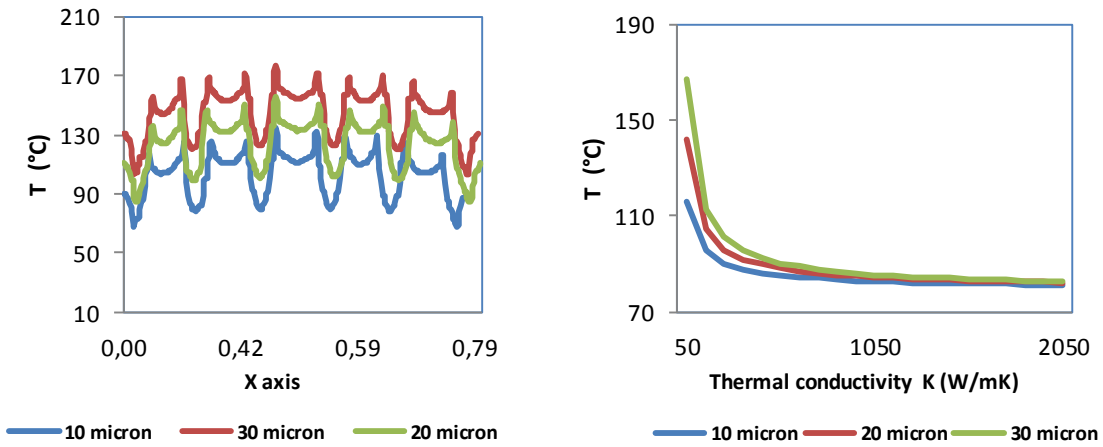

Figure 4: Temperature profile along x axis gained at different bumps heights and with K=60 W/mk. Temperature profile Vs thermal conductivity at the device centre for different bumps' connection height.

Our simulation evidences also that CNT bump width influences heat dissipation ability for low values of thermal conductivity (60 W/m K); after a value of about 1250 W/mk, a different bump's width doesn't change thermal profile.
In order to improve conduction process and prevent risk caused from negative-bias temperature instability a simulation was also performed covering all chip surface with a fine layer of gold. All temperatures are much lower than that measured during previous simulations, see Figure 5. The Au layer results able to reduce the occurrence of peak over-temperature along the chip, increasing the heat dissipation area and improving the dissipation efficiency in a simplest way than the complex 3D CNT architecture reported by Zhang et al. (Zhang et al., 2011).

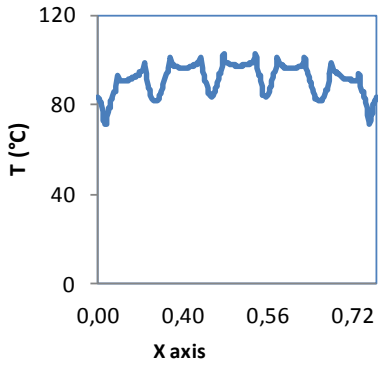

Figure 5: Temperature profile along x axis at bumps heights of 10 µm, with K=60W/mk and Au layer.

For a k value of 300 W/mk, the maximum junction temperature gained in the chip is less than 85°C, see Figure 6. In all the conditions the highest temperatures were reached in the center of the package, likely due to its symmetry. Therefore the central points are the critical ones for reliability issues.
We also tested the introduction of a major number of CNT's bumps with a K value of 300 W/mK, see Figure 7 left side. Increasing bumps number, thermal management results improved, in terms of maximum temperature reached in the device as junction temperature and maximum temperature differences along x axis, see Figure 7 right side.
Considering the case of more devices working together, we performed also simulations in the absence of natural convection towards lateral walls of the device. We found that also in this case CNT's bumps showed improved thermal management performance also if compared with a common flip chip device, with Cu_6Sn_5 solders bumps in a forced convection regime, 1 m/s, of transformer oil at 273 K.

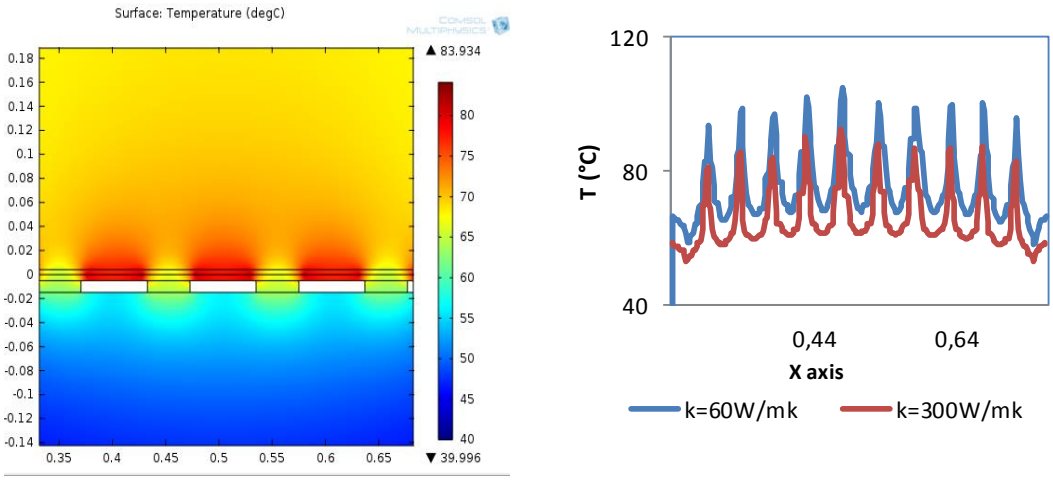

Figure 6: Left side: device Temperature with bumps' connection height of 10 µm and with Au layer Kbumps=300 W/mk. Right side: Temperature profile along x coordinate (bumps height of 10µm).

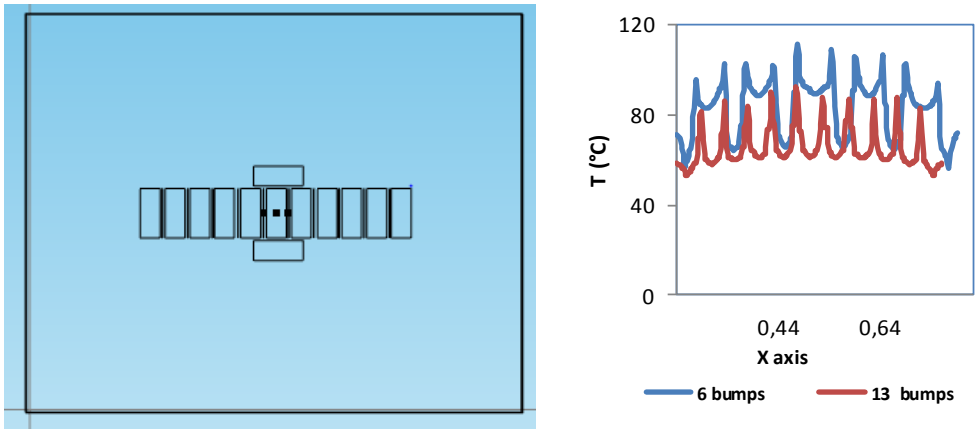

Figure 7: Temperature result differences between 6 and 13 bumps simulations

4. Conclusions

CNTs have been successful grown on a AlN substrate and their conductivity measured with the help of Raman spectra. Simulation results showed significant temperature reduction at lower bumps height and in presence of an Au layer. From the simulations it can be stated that CNT width influences heat dissipation for low values of thermal conductivity (60 W/m K); after a value of about 1250 W/mK, different bump's width doesn't change significantly thermal profile. Increasing bumps number, thermal management is improved. Considering the case of more devices working together, our simulation demonstrate that also in this case the effect of CNT's bumps is helpful. Furthermore, the configuration including CNT bumps gives better results than that obtained using a common flip chip device, with Cu_6Sn_5 solders bumps in a forced convection regime, 1 m/s, of transformer oil at 273 K. The best result was obtained in the configuration with Au layer and 10 μm connection height CNTs, resulting in a better hotspots management.

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