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Fabrication of UV sensing transistor based on transparent polycrystalline zinc oxide thin film using polymeric electrolyte gate dielectric

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Abstract

The fabrication of electric double layer thin film transistors (EDLTFTs) using polymeric electrolyte as gate dielectric on chemically grown polycrystalline ZnO thin film channel has the lower threshold voltage at 0.4 V and the saturation current at 3 μA in the dark. The lower threshold voltage is -1 V and the saturation current is 10 μA in the UV illumination. In the dark and under UV light, the off state I_D is 1 nA and 0.3 μA respectively and under gate and UV illumination the on current shows more than 3 times enhancement. This improvement in photocurrent is due to the combined effect of gate and UV illumination. The field effect mobility of the TFT is 0.06 cm^2/Vs in the dark and 0.16 cm^2/Vs under UV illumination. This increase in mobility under illumination and gate bias is due to the increase in carrier concentration and reduction of charged defects in the channel length.

Keywords
Zinc Oxide, thin film transistor, electric double layer, photocurrent, field effect mobility.

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1 Introduction

Low voltage operation thin film transistor (TFTs) based on wide band gap semiconductor with controllable high carrier density is of considerable interest for a variety of inexpensive electronics and optoelectronic applications [1–3]. Zinc oxide (ZnO) a wide band gap (3.3 eV) direct semiconductor having large exciton binding energy (60 meV) is one of such promising materials for many applications such as ultra mobile PCs, smart windows, transparent tablet and paper thin display etc. [4]. ZnO has many advantages over amorphous silicon base transistor such as high carrier mobility, high optical transparency, mechanical flexibility and processing versatility [5, 6]. High transmittance thin film transistor is becoming an important device in the display industries [7, 8]. One of the big challenges in present transistor technology is to increase the maximum attainable carrier density for high performance of the device. The chemical doping to increase the charge carrier is not suitable due to its unnecessary complexity in the physical properties of the material [9, 10]. Conventional metal dielectric gates have relatively low dielectric constants and have the limitation of charge density accumulation [11]. Therefore, the new idea for realizing the field induced surface charge density in field effect transistor is of great importance and urgency. The recent idea to modify the performance field effect transistor named electric double layer (EDL) have been employed for attaining the high carrier density by using polymeric electrolyte gates [11,12]. An EDL can be considered as a nano-gap capacitor with capacitance higher than that of SiO_2 and Al_2O_3. Previous authors have reported many results that the typical sheet carrier density attainable in conventional metal insulator semiconductor is $<1X10^{13}$ cm^{-2}. That is less than EDL ZnO thin film transistor (TFTs) ($\sim 4X10^{14}$) [11, 13]. In contrast to the above, the combined effect of the gate bias and light in charge accumulation properties at room temperature on the standard oxide semiconductor ZnO have been investigated in few numbers and where this combined effects can be more significant than individual one in polycrystalline ZnO electric double layer thin film transistor (EDLTFTs). Many researchers fabricated TFT using EDL gate dielectric in single crystal or texture film however very few groups reported fabrication of TFT using polymer electrolyte on chemically grown polycrystalline ZnO film for gate controlled UV detection. In this report the gate, controlled TFT based UV detector shows three-order enhancement of drain current near the threshold voltage under UV illuminations. This large enhancement of drain current can be achieved due to the simultaneous generation of charge carrier in the presence of gate bias and UV illumination. For this, we have explored the possibility of fabrication of transparent poly crystalline ZnO TFTs using polymeric electrolyte gate dielectric in which the switching action of the transistor requires ionic motion. Here, our main interest is the control of conductivity of the TFT channel by the modulation of surface charge density using gate bias and UV illumination.

2 Materials and Method

2.1 Preparation of precursor solution and substrate cleaning

Zinc acetate dehydrate $[Zn(CH_3COO)_2.2H_2O)]$ of Sigma Aldrich Company with purity 99.9% was first dissolved in 50 ml of isopropyl alcohol $[(CH_3)_2CHOH]$ of same Sigma Aldrich Company with purity 99.7% . The resultant precursor solution was mixed through a magnetic stirrer at 65°C for 2 hrs. In this experiment, the final white precipitate of precursor is slowly dissolved when this mixture was mixed with diethanolamine (DEA) drop wise. Finally transparent clear solution was obtained as precursor for film coating on glass substrate. The glass substrate was ultrasonically treated for 30 min. in acetone and alcohol and dried on hot plate.

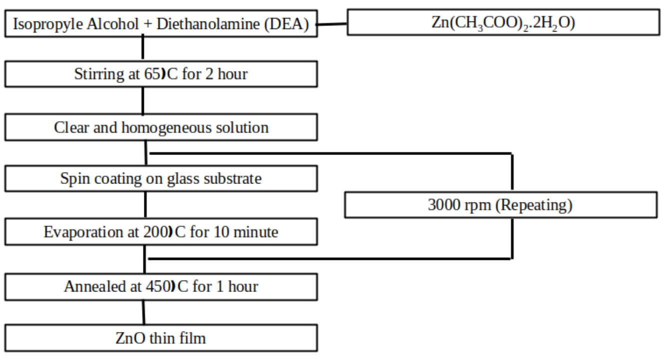


Figure 1: The flow chart of the procedure for preparing ZnO thin films.

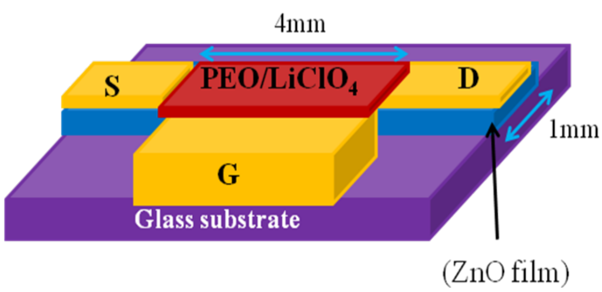
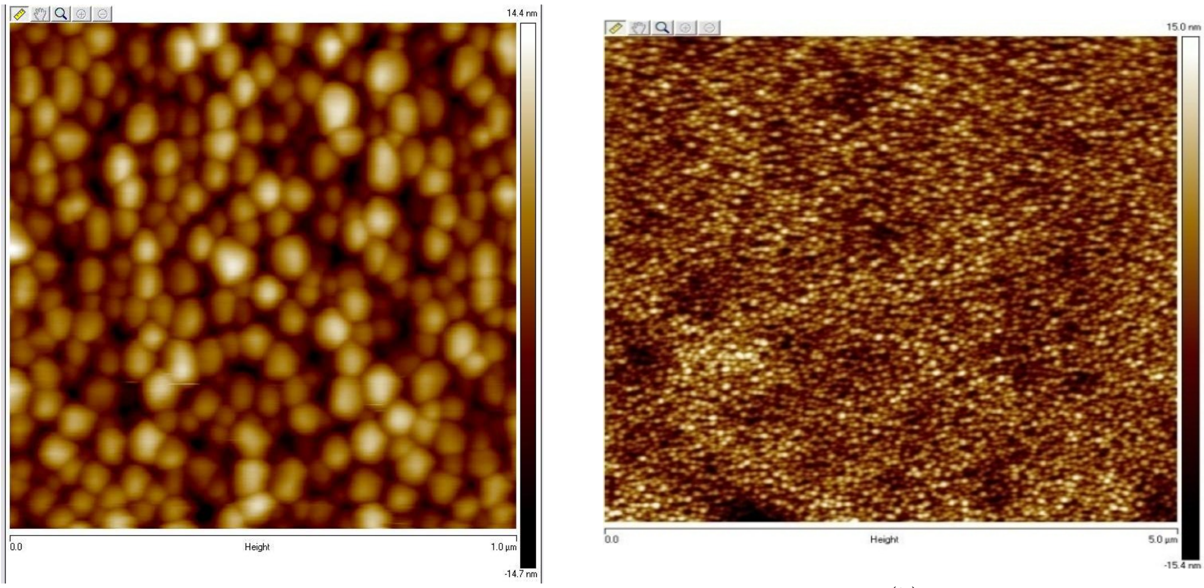


Figure 2: Schematic diagram of polymer electrolyte gated EDLTFTs on ZnO surface.



(a) (b)

Figure 3: AFM images of (a) 1 µm x 1 µm and (b) 5 µm x 5 µm of ZnO film annealed at 450°C.

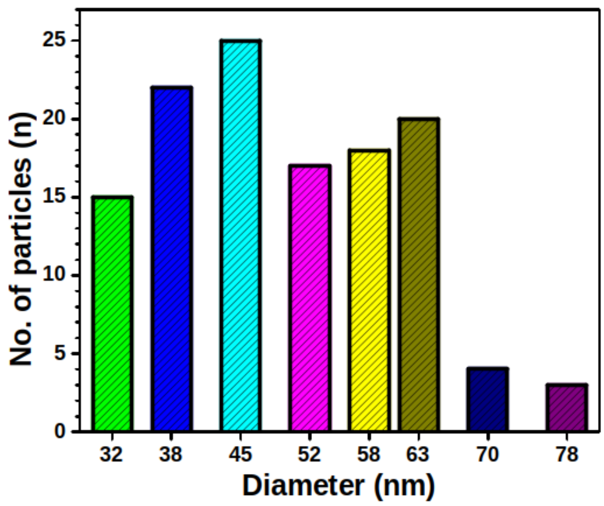


Figure 4: Particles distribution of AFM image in histogram.

2.2 Film growth

The substrate was spin coated with sol at speed 3000 rpm for 30 sec. in air. Each coating on the substrate was heated at 200°C for 10 min. in air. And the same process was repeated for various thicknesses. At last, ZnO thin films on the glass substrate was made ready by annealing at temperature 450°C for 1 hour. The following figure 1 shows the flowchart of the various steps of the ZnO thin film growth.

2.3 Fabrication of EDLTFT ZnO device

Fig. 2 shows the schematic diagram of EDLTFTs. The electrical properties of ZnO TFT were investigated in side-plane gate configuration. Polyethylene oxide: lithium per chlorate (10:1) (PEO/$LiClO_4$) [14] is used for a gate insulator whereas Ti/Au electrodes are evaporated on the film to fabricate source, gate and drain contacts for Field Effect Transistor (FET) structure. The contact pads are designed using hard mask during thermal evaporation. In this device, its channel width to length ratio (W/L) is ≈ 0.25.

3 Results and Discussion

The surface morphology of the chemically grown ZnO film was studied by atomic force microscopy. The phase images in scan range 1 µm x 1 µm and

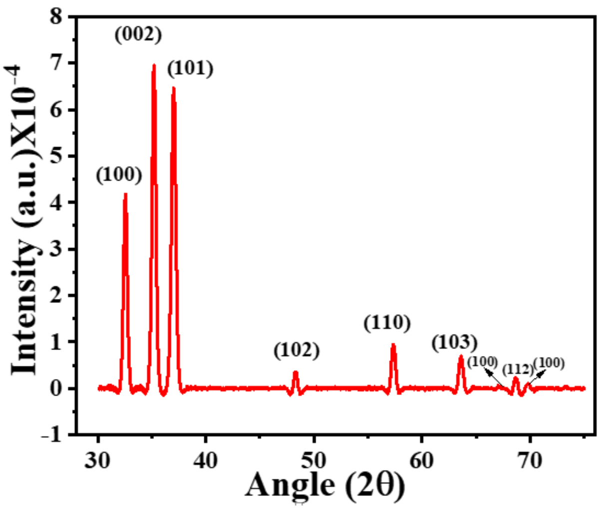


Figure 5: X-ray diffraction pattern of ZnO film

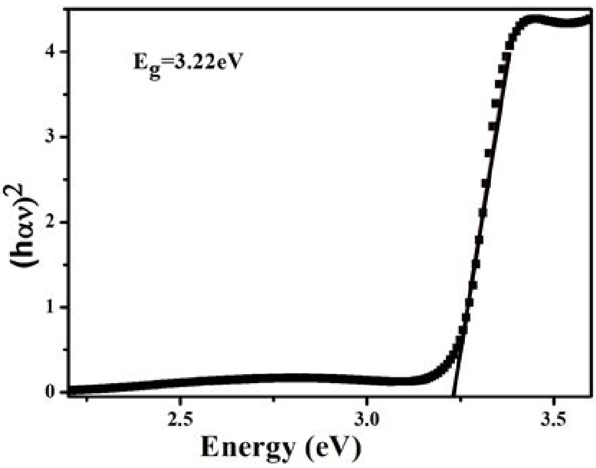


Figure 6: Tauc Plot from UV-Vis analysis of a ZnO thin film to evaluate the band-gap at the X-axis intercept.

5 μm x 5 μm are depicted in fig. 3(a) and (b) respectively. The AFM image analysis also confirmed that thus chemically grown films have some voids and porosity.

The surface roughness of the ZnO film was observed about 5 nm. Fig. 4 depicts the size distribution of the particles within area 1 μm x 0.5 μm. The average grain size was observed about 50 nm.

Fig. 5 illustrates the diffraction pattern of the film. The pattern shows all the promising peaks for different angle of diffraction. This indicates that the polycrystalline nature of the film. Here it is observed that there are three main peaks in the X-ray diffraction pattern which are (100), (002) and (101) which indicate that the film are polycrystalline and randomly orientated [10, 15]. The polycrystallinity is expected due to the lack of epitaxial relationship between ZnO and the glass substrate. Further the low deposition temperature to suppress the columnar growth also lead to polycrystallinity in the ZnO film [16]. The most preferential growth direction is along (002). The c/a ratio of the film is observed to be 1.6. Experimental value is consistent with the theoretical value.

Fig. 6 shows Tauc plot from UV-Vis analysis of ZnO thin film to evaluate the band-gap after taken the absorption spectra of the film. The absorption of ZnO film was observed in UV region. In the spectra, sharp absorption occurs around 385 nm. The absorption edge corresponds to the intrinsic band gap of the ZnO. The information about the band gaps were obtained by analyzing dependence of the absorption coefficient on photon energy in the high absorption region. The optical band gap of the film was determined from the absorption spectra by the

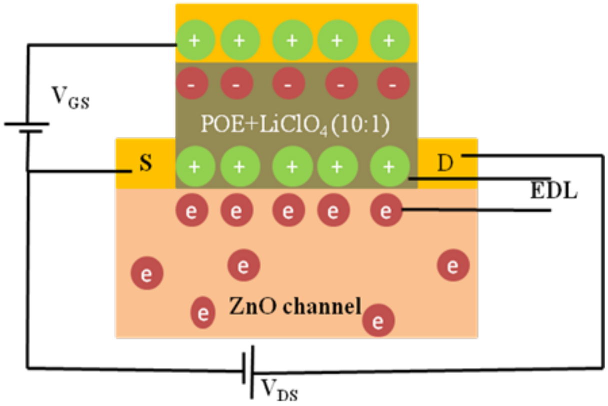


Figure 7: Schematic illustration of electric double layer on ZnO channel.

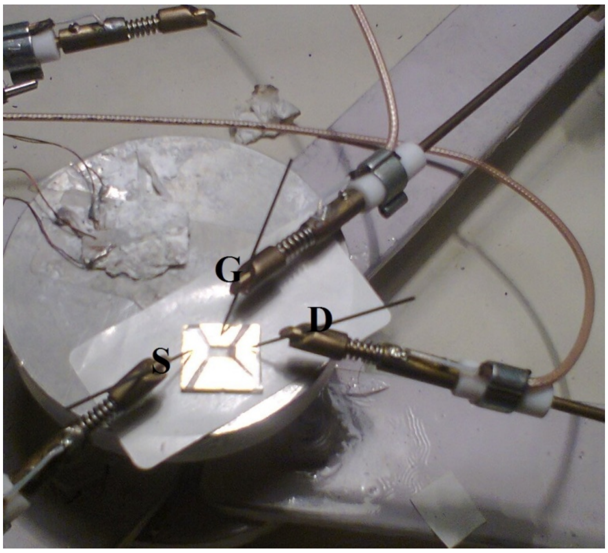


Figure 8: Sample on probe station.

using the following Tauc relation [17–19]

$$(\alpha h\nu) = A(h\nu - E_g)^m \quad (1)$$

where A is energy independent constant, h is plank's constant, Eg is the optical band gap and m is a constant that determines the type of transition. Its value is taken 2 for indirect and $\frac{1}{2}$ for direct transition. The band gap of the film was observed 3.22 eV.

3.1 Characterization of electric double layer (EDL) ZnO TFT

In this study, carriers are accumulated at source-drain channel with an EDL by the application of the gate voltage. Fig. 7 illustrates the formation of the electric double layer by using polymer electrolyte on the ZnO channel. When a positive bias is applied to the gate electrode, the mobile anion of the electrolyte move towards the positively charged electrode whereas the cation is moved towards the channel gate insulator interface. Thus electric double layers are formed at two interfaces of the Polymeric electrolyte gate material. These layers act as a nano-gap capacitors [1, 11] with high capacitance more than the conventional metal dielectric gate capacitance and able to induce the large surface charge density [14, 20–22]. The principal aim of using the polymer electrolyte is to enhance and control the charge carrier density in channel layer.

The figure 8 shows the sample mounted on four probe station to the transistor characteristics in air. In this figure, S represents the source, D represents the drain and G represents the gate in TFT of zinc oxide. The transfer characteristic of EDLTFTs is measured by using Kiethly source meter 2400 at room temperature. The EDLTFTs operates as an n-channel enhancement mode device i.e. a positive gate voltage is required to induce the conducting channel.

Fig. 9 shows transfer curve (gate voltage V_{GS} versus drain current I_D) measured at a drain voltage V_{DS} of 10 V. At low gate voltage (<1 V), the

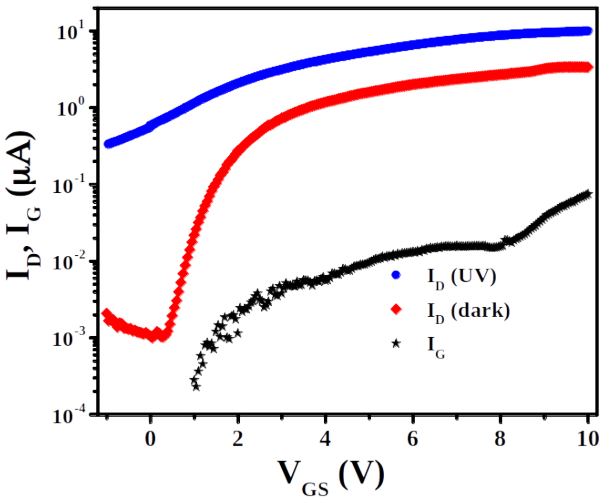


Figure 9: Transfer characteristic (I_D, I_G vs. V_{GS} in dark and UV illumination).

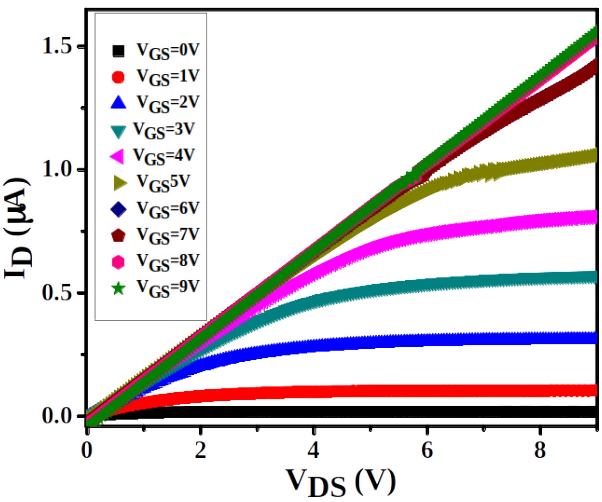


Figure 10: Drain characteristic with applied voltage V_{GS} 0 to 9 V under dark (with scan speed 0.5 V/min.)

channel is highly resistive, the value of resistivity is observed ≈ 3×10^6 Ωcm. We observed the linearly increase in I_D above the thresh hold voltage (i.e. -1 V for UV and 0.4 V for dark). At low gate bias voltage, the gate current (I_G) is very low or negative which is not shown in the graph. As the gate bias voltage increases positively, the I_G also increases but still the value of I_G is almost less than 3 order magnitude of the drain current at on state. This confirms that the performance of the device is not affected by the leakage current and also clearly demonstrates the n-type FET action. Above the V_{GS} >8 V, the I_G starts to increase abruptly which notifies leakage I_G and leads to change the drain current. This suggests that the polymer electrolyte gate dielectric is not suggestable to bias above 8V. The maximum current (I_D = 3 µA) is obtained at V_{GS}= 10 V in the dark with width to length ratio (≈ 0.25) of the device. The role of gate bias voltage is to increase the no. of charge carriers, therefore the corresponding drain current is also increased without any significant change in gate current. This phenomenon occurs with increasing the gate voltage up to certain limit up to 8 V and saturated. That means no further change in carrier density in channel length due to the gate electric field.

The on off ratio of the device is 10^3 and 30 in dark and UV illumination respectively. The lower threshold voltage at 0.4 V and saturation current at 3 µA is observed in dark, whereas the lower threshold voltage at -1 V and saturation current at 10 µA is observed in UV illumination. The off state I_D is 1 nA in dark and 0.3 µA in UV illumination. This large change in off state current during illumination is due to the band edge absorption of the ZnO nanostructure thin film [14, 20, 21, 23]. The important observation of the experiment is the enhancement of the photocurrent under UV illumi-

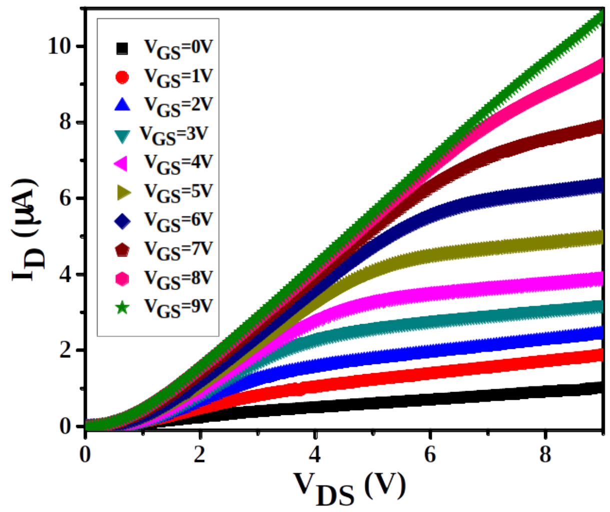


Figure 11: Drain characteristic with applied voltage V_{GS} 0 to 9 V under UV illumination (with scan speed 0.5 V/min.)

nation due to the combined effect of gate and illumination. Under gate and UV illumination, the on current shows more than 3 times enhancement and saturates about 10 µA. Therefore, the charge carrier is increased by more than 3 times with combined effect of gate and UV light in on state. The charged defects states are neutralized by these field induced and light generated charge carriers which leads to enhance the filed effect mobility in the channel [21, 24, 25].

The transconductance (g_m) of the EDLTFTs is calculated from an (I_D) -V_{GS} curve by using the following equation in active mode or saturation regime ($V_{GS} > V_{th}$ and $V_{DS} \geq (V_{GS} - V_{th})$ [2].

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = (W/L) C_{in} \mu_{FE} V_{GS} \quad (2)$$

Here W and L are the length and width of the channel, C_{in} is the capacitance of the electrolyte ZnO interface and μ_{FE} is the field effect mobility. Transconductance (g_m) of 4.5x10^{-7} S is obtained in the EDLTFTs with a source drain voltage of 10 V and gate bias 5 V in dark. In UV illumination, it is observed 1.21x10^{-6} S. From above calculation, the field effect mobility of the TFT in dark is observed 0.06 cm^2/Vs and that of under UV illumination is 0.16 cm^2/Vs. This increase in mobility under illumination is due to the increase in carrier concentration in the channel length.

Fig. 10 and 11 shows the drain characteristatic of EDLTFTs in dark and UV illumination respectively. The output characteristatic showed the typical saturation behaviour at low bias voltage i.e. V_{GS}<5 V in dark and above that gate bias voltage, the drain current is linear. However, under UV illumination, the drain current is not perfectly saturated even at low gate voltage i.e. at V_{GS}<8 V. This unsaturated behiour of drain current is due to the generation of huge charge carriers under band gap illumination. The ohmic behaviour emerged for V_{GS}>5 V in dark and V_{GS}>8 V under UV illumination.

4 Conclusion

The overall results and discussions show possibility of fabrication of EDLTFTS by using polymeric electrolyte as gate dielectric on chemically grown polycrystalline intrinsic ZnO thin film channel. In the dark, the lower threshold voltage is 0.4 V, and the saturation current is 3 µA, whereas in UV illumination, the lower threshold voltage is -1 V, and the saturation current is 10 µA. The high on off ratio (≈10^3 in dark and 30 in UV illumination) is achieved in the experiment by in plane gate configuration. In the dark and under UV light, the off state I_D is 1 nA and 0.3 µA, respectively. This large change in off state current during illumination is due to the band edge absorption of the ZnO nanostructure thin film. In addition to this, under band gap wavelength illumination, the on current shows more than three times enhancement showing that the device can be controlled electrically by a gate as well as UV light. The important observation of the experiment is the improvement in photocurrent under UV light brought on is by the combined effects of the gate and UV illumination. The field effect mobility of the TFT is 0.06 cm^2/Vs in the dark and 0.16 cm^2/Vs under UV illumination. The increase in carrier concentration in the channel length is the cause of the increased mobility under illumination.

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