Numerical Simulation of Nanoscale Double-Gate MOSFETs

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The further improvement of nanoscale electron devices requires support by numerical simulations within the design process. After a brief description of our SIMBA 2D/3D-device simulator, the results of the simulation of DG-MOSFETs are represented. Starting from a basic structure with a gate length of 30 nm, the model parameters were calibrated on the basis measured values from the literature. Afterwards variations in of gate length, channel thickness and doping, gate oxide parameters and source/drain doping were made in connection with numerical calculation of the device characteristics. Then a DG-MOSFET with a gate length of 15 nm was optimized. The optimized structure shows suppressed short channel behavior and short switching times of about 0.15 ps.

Keywords: Device simulation, semiconductor devices, double-gate MOSFET.

Notation

p, n	hole and electron density (cm^{-3})
φ	electrostatic potential (V)
N_A, N_D	ionized donor and acceptor density (cm^{-3})
ε_s	permittivity of semiconductor ($AsV^{-1}m^{-1}$)
q	elementary charge (As)
$\boldsymbol{J}_p, \boldsymbol{J}_n$	current densities (Acm^{-2})
R, G	recombination and generation rate ($cm^{-3}s^{-1}$)
μ_p, μ_n	carrier mobilities ($cm^2V^{-1}cm^{-1}$)
λ_p, λ_n	quantum correction potentials (V)
Θ_p, Θ_n	band parameters (V)
D_p, D_n	diffusion coefficients (cm^2s^{-1})
T_p, T_n	carrier temperatures (K)
k_B	Boltzmann constant (eVK^{-1})
$\boldsymbol{S}_p, \boldsymbol{S}_n$	energy flux densities (Wcm^{-2})
$\boldsymbol{E}$	electric field strength (Vcm^{-1})
T_L	lattice temperature (K)
τ_{wp}, τ_{wn}	energy relaxation times (s)
m_p, m_n	carrier effective masses (kg)
$\hbar$	reduced Planck's constant (Js)
γ_p, γ_n	quantum correction coefficient
κ_p, κ_n	thermal conductivities ($WK^{-1}cm^{-1}$)

1 Introduction

Double-Gate (DG) MOSFETs are considered to be a promising candidate for nanoscale CMOS. The International Technology Roadmap for Semiconductors (2005 Edition) predicts printed gate lengths up to 15 nm for the next ten years. For these gate lengths conventional MOSFETs are limited due to different short channel effects. On the other hand structures with two gates and an extremely thin body demonstrate better control of the gate region and consequently suppression of short channel effects.

Numerical device simulation is an important procedure for the design and optimization of novel semiconductor devices. Some advantages are that the electrical behavior iscalculated before the fabrication process, non-measurable inner-electronic values can be calculated and visualized, and cost effectiveness due to diagnosis/fault-detection in the technological process.

2 Simulation models

Quantum hydrodynamic (QHD) models, which are based on a quantum fluid dynamic model, offer new ways to understand and design quantum sized semiconductor devices. The advantage of this model is its macroscopic character, which enables us obtain description without knowing of quantum mechanical details like the initial wave function [1], [2], [3]. The classical hydrodynamic (HD) model for semiconductor device simulation can be extended by expressions in the transport equations and in the energy balance equations. These describe an internal quantum potential in the transport equation as well as a quantum heat flux in the energy balance equation. These additional terms in the classical hydrodynamic model allow us to describe the continuous electron and hole distribution in a semiconductor device, accumulations of carriers in potential wells and resonant tunneling of carriers, respectively. The standard model for universal device simulations is the drift-diffusion (DD) model, which can be derived from the above mentioned model [4].

Basic equations of the QHD model are the Poisson equation

$$\nabla\left(\varepsilon_s \nabla(\varphi)\right) = -q\left(p - n + N_D - N_A\right) \qquad (1)$$

continuity equations (index p: holes, index n: electrons)

$$\nabla \cdot \boldsymbol{J}_p = -q\left(R - G + \frac{\partial p}{\partial t}\right) \qquad (2)$$

$$\nabla \cdot \boldsymbol{J}_n = -q\left(R - G + \frac{\partial n}{\partial t}\right) \qquad (3)$$

transport equations

$$\boldsymbol{J}_p = -q\,p\,\mu_p \nabla(\varphi - \lambda_p\Theta_p) - D_p q \nabla(p) - k_B p\,\mu_p \nabla(T_p) \qquad (4)$$

$$\boldsymbol{J}_n = -q\,n\,\mu_n \nabla(\varphi - \lambda_n\Theta_n) - D_n q \nabla(n) + k_B n\,\mu_n \nabla(T_n) \qquad (5)$$

energy balance equations

$$\nabla \cdot \boldsymbol{S}_p = \boldsymbol{J}_p \cdot \boldsymbol{E} - \frac{3}{2} k_B p \frac{T_p - T_L}{\tau_{wp}} - \frac{3}{2} k_B \frac{\partial}{\partial t}(pT_p)$$

$$- \frac{3}{2} k_B T_p (R-G) - \frac{1}{2} q \lambda_p \left(\frac{p}{\tau_{wp}} - (G-R) \right) - \frac{1}{2} q \frac{\partial}{\partial t}(p\lambda_p) \tag{6}$$

$$\nabla \cdot \boldsymbol{S}_n = \boldsymbol{J}_n \cdot \boldsymbol{E} - \frac{3}{2} k_B n \frac{T_n - T_L}{\tau_{wn}} - \frac{3}{2} k_B \frac{\partial}{\partial t}(nT_n)$$

$$- \frac{3}{2} k_B T_n (R-G) + \frac{1}{2} q \lambda_n \left(\frac{n}{\tau_{wn}} - (G-R) \right) + \frac{1}{2} q \frac{\partial}{\partial t}(n\lambda_n) \tag{7}$$

energy flux density equations

$$\boldsymbol{S}_p = -\kappa_p \nabla(T_p) + \frac{5}{2} \frac{k_B}{q} T_p \boldsymbol{J}_p + \frac{3}{2} \lambda_p \boldsymbol{J}_p \tag{8}$$

$$\boldsymbol{S}_n = -\kappa_n \nabla(T_n) - \frac{5}{2} \frac{k_B}{q} T_n \boldsymbol{J}_n + \frac{3}{2} \lambda_n \boldsymbol{J}_n \tag{9}$$

and equations for the quantum correction potential

$$\lambda_p = -\frac{\gamma_p \hbar^2}{6 m_p q} \frac{\nabla^2 \sqrt{p}}{\sqrt{p}} \tag{10}$$

$$\lambda_n = \frac{\gamma_n \hbar^2}{6 m_n q} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \tag{11}$$

Further approaches are necessary for carrier mobilities, generation and recombination rates, diffusion coefficients and energy relaxation times, which are almost material dependent. Equations (1) to (11) are solved self-consistently for the variables ($\varphi, p, n, T_p, T_n, \lambda_p, \lambda_n$). If equations (10) and (11) are neglected, i. e., for $\lambda_p = \lambda_n = 0$, the QHD model can be reduced to the conventional hydrodynamic (HD) model. If the carrier temperatures are set to lattice temperature and equations (6) to (9) are neglected, the quantum drift diffusion (QDD) model and additionally for $\lambda_p = \lambda_n = 0$ the conventional drift diffusion (DD) model can be obtained. Solutions of the equations are achieved by a successive algorithm (the so
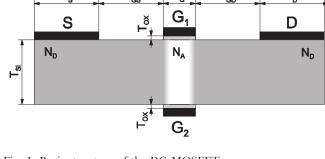

Fig. 1: Basic structure of the DG-MOSFET

called Gummel algorithm). For solving the partial differential equations a box method is used. The resulting non-linear equation systems are solved by the NEWTON-method and the corresponding linear equation systems by preconditioned gradient methods. All models are implemented fully three--dimensionally in the SIMBA program system [5], [6].

3 Basic structure simulation and verification

The starting point for the simulations is a basic structure represented in Fig. 1, as a functionally relevant detail of the real device. The different parameters are assumed as follows:

- gate length $L_G = 30$ nm,
- source/drain lengths $L_S = L_D = 100$ nm,
- gate-to-source and gate-to-drain distances $L_{GS} = L_{GD} = 100$ nm,
- silicon film thickness $T_{Si} = 20$ nm,
- gate oxide thickness $T_{ox} = 2$ nm,
- channel doping $N_A = 1 \times 10^{16}$ cm^{-3},
- source/drain doping $N_D = 3 \times 10^{20}$ cm^{-3}.

The simulated output characteristics drain current I_D versus drain-to-source voltage V_{DS} are plotted in Fig. 2 for
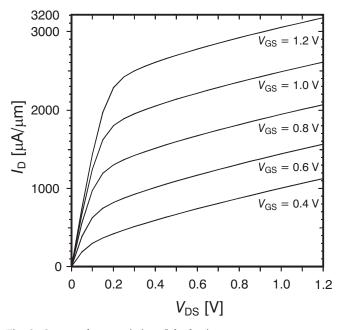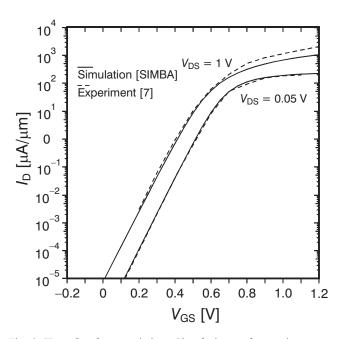

Fig. 2: Output characteristics of the basic structure

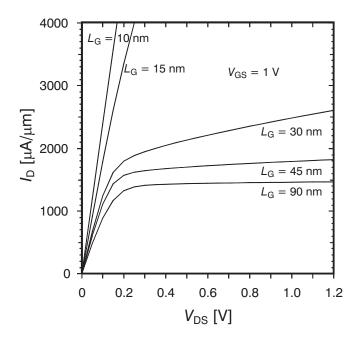Fig. 3: Transfer characteristics – Simulation and experiment

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Fig. 4: Output characteristics at different gate lengths

Fig. 5: Transfer characteristics at different gate lengths

different gate-to-source voltages V_{GS}. Verification of the simulation results and calibration of the model parameters were done by comparison with experimental values from [7]. A structure similar to Fig. 1 with $L_G = 45$ nm, $T_{ox} = 2.5$ nm, $N_D = 2 \times 10^{20}$ cm^{-3} was simulated and compared with the measured values. The results represented in Fig. 3 show good agreement. A further successful verification was done by results from [8].

4 Parameter variation and optimization

To study the influence of the structure parameters on the electrical device characteristics, various parameters are modi-
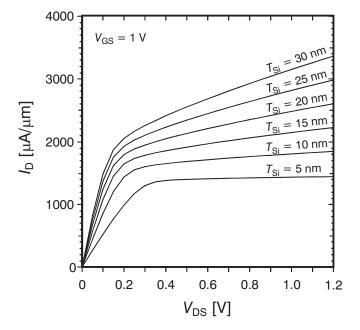
fied. Figs. 4 and 5 depict the output and the transfer characteristics at different gate lengths. At shorter gate lengths a threshold voltage roll off can be observed as a typical short channel effect in the particular pinch-off behavior disappears for $L_G < 30$ nm. At the same time, the drain saturation current increases strongly.

Variation results of the silicon film thickness are represented in Fig. 6. Thicker channels lead to larger drain currents, and also to a displacement of the threshold voltage toward smaller values. Therefore the film thickness should be not greater than 20 nm. Thinner gate oxides result in increasing drain currents (Fig. 7) and transconductances, and in a better pinch-off behavior. Therefore the smallest possible oxide thickness should be applied.
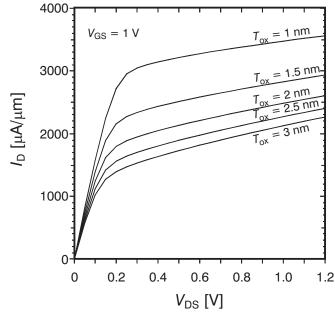

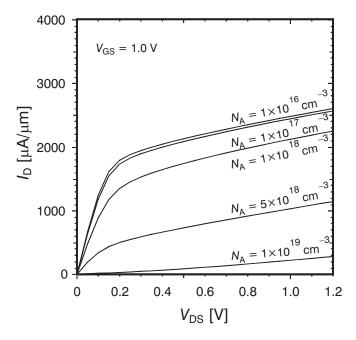Fig. 6: Output characteristics at different channel thickness

Fig. 7: Output characteristics at different gate oxide thickness
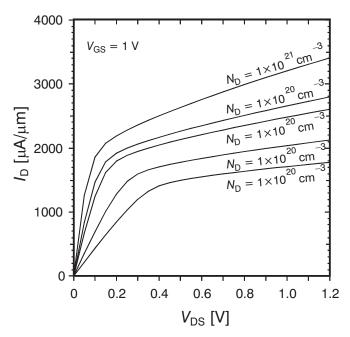
Fig. 8: Output characteristics at different channel doping

Fig. 10: Output characteristics of the optimized structure

Fig. 9: Output characteristics at different source/drain doping

Fig. 11: Transfer characteristics of the basic and the optimized structure

Variation of the channel doping causes a decrease in the drain current for doping densities greater than 10^{17} cm^{-3} (Fig. 8). The threshold voltage is strongly influenced by doping changes. For optimization of the structures, channel doping can be used to adjust the required threshold voltage. The source/drain doping should be high enough to reduce the series resistances, whereas the dopant diffusion into the channel has to be minimized to prevent short channel effects. In this case rapid thermal annealing processes are an essential equirement. Fig. 9 shows the corresponding output characteristics.

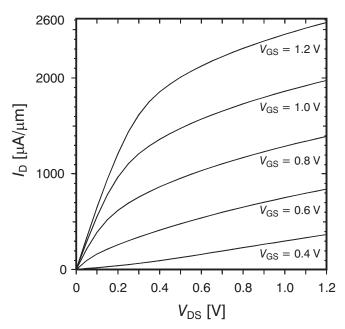The knowledge gained from the different variations was used for the design of an optimized structure. A minimal technologically practicable gate length of $L_G = 15$ nm and a gate oxide thickness of $T_{ox} = 1.5$ nm are specified. Further objectives are threshold voltage of $V_{Th} = 0.1$ V, large drain saturation current and improved dynamical behavior. After several iterations the further parameters are determined as follows: $T_{Si} = 3$ nm, $N_A = 2.8 \times 10^{19}$ cm^{-3}, $N_D = 7 \times 10^{20}$ cm^{-3}. The resulting output characteristics are represented in Fig. 10. Fig. 11 compares the transfer characteristic of the optimized and basic structure. An enlarged drain current as well as an improved transconductance can be observed.

To determine the dynamical behavior, the gate-to-source voltage was switched from 0 V to 1 V to find the turn-on time (t_{ON}) and from 1 V to 0 V to find the turn-off time (t_{OFF}).
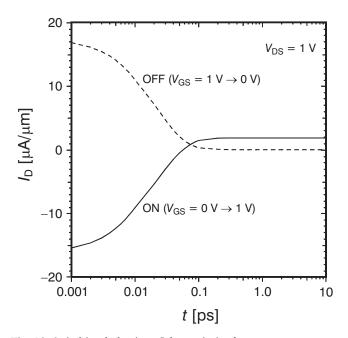
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Fig. 12: Switching behavior of the optimized structure

Fig. 12 shows the time response of the drain current. This provides the switching time of $t_{ON} = t_{OFF} = 0.15$ ps. Compared with the basic structure the switching times are reduced by a factor of 0.6, primarily due to the structure reduction.

5 Conclusion

The scaling down of planar bulk MOSFETs according the International Technology Roadmap for Semiconductors requires new structures such as multiple-gate MOSFETs A promising way to this is with the use of double-gate transistors. The implementation will be challenging, with numerous new and difficult issues. In this case numerical device simulation is essential. Variations of different structure parameters have been carried out to calculate the influence on device characteristics. Based on these results an optimized structure with a gate length of 15 nm was created. The optimized structure shows suppressed short channel effects and switching times of about 0.15 ps.

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