RESEARCH ARTICLES

The new CAS-DIS digital ionosonde

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ABSTRACT

A high quality digital ionosonde called the Chinese Academy of Sciences digital ionosonde (CAS-DIS) has been developed for investigations of the ionosphere. Two important features are used for the CAS-DIS; first, the technique of analog down-conversion has been replaced by the new approach of digital down-conversion technology. Secondly, to solve the problem of large instantaneous receiving bandwidth in digital receivers, an analog narrowband tracking filter is used for the CAS-DIS. The center frequency of the filter tracks the carrier frequency transmitted in real-time, to ensure that the frequency components are filtered out of the effective bandwidth. This report describes the system architecture of the CAS-DIS, its main features, and its test results for ionosphere detection.

1. Introduction

An ionosonde is an instrument for the recording of electron density profiles of the ionosphere. Basically, it works on the principle that a radio wave will be totally reflected if the radio frequency is equal to the characteristic frequency of the ionosphere, which depends on the plasma frequency, $f_p = (80.5N)^{1/2}$ Hz, where N is the electron density in electrons/m^3. By the adjustment of the transmitted frequency from 1 MHz to 30 MHz and the measurement of the time delay of any echo, an ionosonde can provide a profile of electron density *versus* height.

The most widely used ionosondes are IPS-42, AIS-INGV, CADI and Digisonde-4D. The AIS-INGV adopts a receiving heterodyne system that is based on multiple analog conversions. To accomplish these conversions, three local oscillators were devised. Conversion filters have to be added before and after, to clean the noise from the signal [Zuccheretti et al. 2003]. The Digisonde-4D uses down-converter and up-converter integrated-circuit chips, the Graychip GC5016 and Analog Devices AD9857, to implement the classic functions of radio transmitters and receivers by numeric techniques. However, the direct-to-radio frequency (RF) technology was not considered for the high-frequency receiver design for the Digisonde [Reinisch et al. 2009]. In general, the techniques of analog I/Q demodulation with analog-to-digital conversion of the baseband are used in conventional ionosonde receivers.

The availability of high-speed analog-to-digital converters (ADCs), that can directly sample receiver RF signals has resulted in the almost universal adoption of digital receiver architectures over conventional analog I/Q demodulation. A new ionosonde, called the Chinese Academy of Sciences digital ionosonde (CAS-DIS), has been developed in the Key Laboratory of Electromagnetic Radiation and Sensing Technology, Institute of Electronics, Chinese Academy of Sciences (Beijing, China). For the CAS-DIS digital receiver, a single ADC is used to digitize the received RF signal, and digital-signal processing is used to perform the down-conversion to I and Q baseband signals. To solve the problem of saturation caused by interference, an analog narrowband tracking filter is used at the front end of the digital receiver. Moreover, the implementation of a digital down-converter (DDC) is based on a field-programmable gate array (FPGA) platform, and the output of the I and Q data are 32-bit width, which greatly enhances the dynamic range of the receiver. The digital waveform is also implemented in the FPGA using a direct digital synthesizer (DDS), which decreases the dimension and power consumption of the system. These designs improve the flexibility of the CAS-DIS. To upgrade the function of the system, the software of the FPGA just needs to be reloaded, with no need to change the hardware of the system.

2. System design of the CAS-DIS

2.1. General description and specifications

The range resolution of an ionosonde can be significantly improved by the use of very short pulses. However, this use of short pulses decreases the average transmitted power, which is directly linked to the signal-to-noise ratio (SNR) of the receiver. It is often desirable to increase the pulse width to increase the average transmitted power while simultaneously maintaining an adequate range resolution,

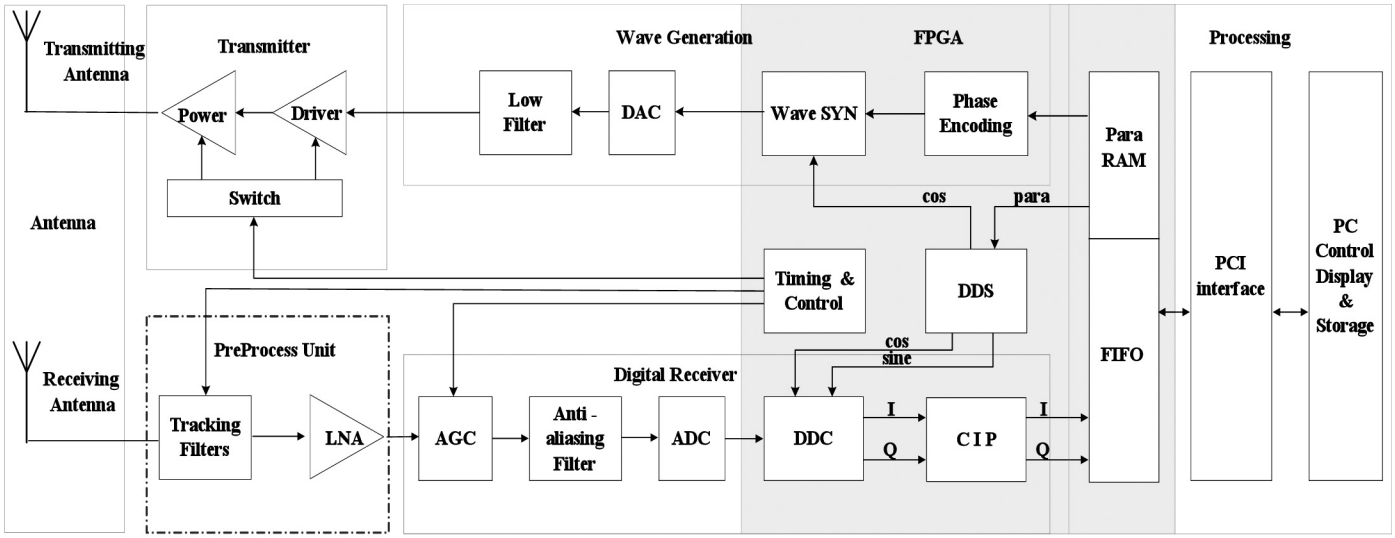

Figure 1. Block diagram of the CAS-DIS.

which can be made possible by using the pulse compression technique [Mahafza 2000]. Phase encoding and the digital pulse compression technique are used for the CAS-DIS. The critical factor in the use of phase encoding and the pulse compression technique for an ionosonde is the correlation properties of the internal phase code [Bianchi et al. 2003]. Complementary sequences consist of two codes of the same length, N, the aperiodic autocorrelation functions of which have side-lobes that are equal in magnitude but opposite in sign. The sum of the two autocorrelation functions has a peak of 2N and a side-lobe level of 0; hence, the complementary sequences were the best choice for the new ionosonde design. Moreover, there are other kinds of code that can be used for the CAS-DIS, such as 13-bit Barker code.

The new design of the CAS-DIS is based on the concept of software-defined radios, which can be divided into five parts. Specifically, these parts are the timing and control unit, the transmitting path, the receiving path, the antenna system, and the pulse compression processing unit. Figure 1 shows the block diagram of the CAS-DIS.

The CAS-DIS works in the frequency range of 1 MHz to 26 MHz, with steps of 50 kHz, which can detect distances from 90 km to 990 km with a range resolution of 5 km. Two kinds of code can be selected: 16-bit complementary code, and 13-bit Barker code. The maximum transmitted power is about 600 W. The specifications of the CAS-DIS are given in Table 1.

Symbols	Description
Frequency range	1-26 MHz
Height range	90 km~990 km
Range resolution	5 km, complementary code 6 km, Barker code
Tx power	600 W (maximum peak)
Frequency point num.	500 (maximum)
Code type	16-bit complementary, 13-bit Barker
ADC sampling rate	60 MHz
ADC bit number	14-bit
Receiver sensitivity	-120 dBm @ 150 kHz
Antenna	Delta antenna

Table 1. The CAS-DIS specifications.

2.2. Timing and control unit

The whole system of the CAS-DIS is controlled by the timing and control unit, as shown in Figure 1. This timing and control unit works as follows: when the configuration parameters are downloaded through the peripheral component interconnect interface to the FPGA internal parameter random-access memory, the software on the PC will generate a corresponding reset signal. Once the timing and control unit detects the reset signal, the control logic will generate the timing and control signals, according to the configuration parameters.

2.3. Transmitting path

As shown in Figure 1, the transmitting path of the CAS-DIS contains the wave generation and the transmitter. The wave generation is composed of several parts, including the DDS unit, the phase-encoding unit, the wave SYN unit, the digital-to-analog converter, and the low-pass filter unit. The details of each of these parts are given in the following.

The DDS produces waveforms by using digital techniques, and provides significant improvements in stability, precision, agility and versatility over analog techniques. The DDS unit in the CAS-DIS generates the sine and cosine signals from 1 MHz to 26 MHz, and the frequency of the DDS can be tuned to be fixed or to be modified in real-time by the pa-

rameters from the PC. The initial phase of the DDS in each pulse repetition frequency (PRF) should be fixed; e.g., 0° or ±90°, and this parameter is used in the coherent integration.

Signals generated by the DDS unit are used as the carrier signal of the transmitted pulse, and a copy of the signals is sent to the receiving path as the local oscillator signals of the DDC. For the CAS-DIS, the DDS unit is implemented by the logic resources within the FPGA. The sampling rate of the DDS is 60 MHz, and the output signals of the phase accumulator and the DDS are 28-bit and 14-bit, respectively. Therefore, the spurious free dynamic range of the DDS can be up to 82 dB, and the adjusting resolution is about 0.25 Hz. The block diagram of the DDS is shown in Figure 2.

The phase-encoding unit generates the 16-bit complementary code or 13-bit Barker code, to modulate the carrier signal generated by the DDS unit. When the 16-bit complementary code is used in the CAS-DIS, the length of a single chip, Ts, is about 33.33 μs, which corresponds to a bandwidth of 30 kHz. In this case, the range resolution is 5 km and the pulse width of the transmitted pulse, T, is 16× the Ts, which is about 533.33 μs. When the 13-bit Barker code is used, the Ts is 40 μs, which corresponds to a bandwidth of 25 kHz. In this case, the range resolution is 6 km, and the duration of T is 520 μs.

The signals of the DDS are modulated with the code by the phase-encoding unit in the wave SYN unit. After it is filtered by the low-pass filter with a bandwidth of 27 MHz, the modulated signal is converted into an analog signal by a digital-to-analog converter, with the output amplitude of 1Vp-p, as shown in Figure 1.

The modulated signal of the digital-to-analog converter can be amplified to 600 W when it is fed to the antenna by the transmitter, as in Figure 1. The transmitter has two stages, known as the driver stage and the power stage. The signal with the level of 1Vp-p from the wave-generation unit can be amplified to about 50Vp-p by the driver stage, and amplified to 500Vp-p by the second stage of the transmitter. Whether the transmitter is on or off is controlled by signals from the timing and control unit.

2.4. Receiving path

The receiving path is comprised of the preprocessor unit, the automatic gain control (AGC), the anti-aliasing filter, the ADC, the DDC, the coherent integration processor, and the first-in, first-out unit. Of these, the DDC, the coherent integration processor, and the first-in, first-out unit are implemented within FPGA, as shown in Figure 1.

The signal received by the receiving antenna is amplified by the preprocessor unit and sent to the indoor receiver. In the short-wave band, the output voltage is proportional to the dimension of the receiving antenna. As a result, when a small antenna is used, the output of the receiving antenna is usually low. To transfer the signal from the receiving antenna to the indoor receiver without much loss of SNR, a low-noise amplifier should be placed at the stage of the receiving antenna output; the gain of the low-noise amplifier is about 16 dB for the CAS-DIS. In addition, because the CAS-DIS works in the short-wave band and there are a large number of broadcasting stations, to avoid saturation of the receiver caused by interference from the radio signals, an analog narrowband tracking filter is applied at the front end of the receiver [Bibl 1998].

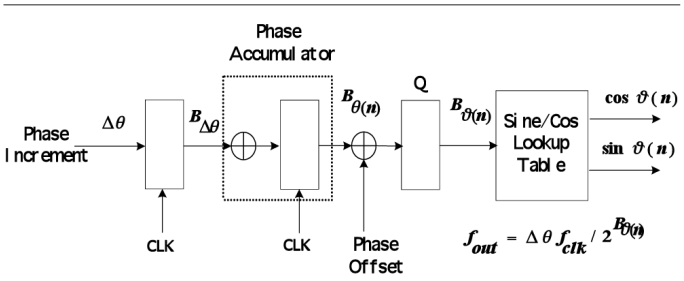

Figure 2. Block diagram of the DDS in the transmitting path.

For the CAS-DIS, the center frequency of the narrowband tracking filter and the carrier frequency of the transmitted RF signal are synchronized. These are controlled by parameters that are reloaded from the parameter random-access memory at the beginning of each PRF. For the CAS-DIS, the frequency range of 1 MHz to 30 MHz can be divided into two bands, of 1 MHz to 1.6 MHz, and 1.6 MHz to 30 MHz. Within the range of 1 MHz to 1.6 MHz, the input of the filter is directly connected to the output, due to the size limitation of the device. The frequency range of 1.6 MHz to 30 MHz can be divided into 750 frequency bands with a -3 dB pass bandwidth of <2.4%. Figure 3 shows the test results of the frequency response of the narrowband tracking filter. The narrowband tracking filter is an effective component to improve the performance of the CAS-DIS if there is interference in the receiving bandwidth.

For the CAS-DIS, the preprocessor unit is designed to be an independent component that can be added or removed freely without affecting the other parts of the system. If the

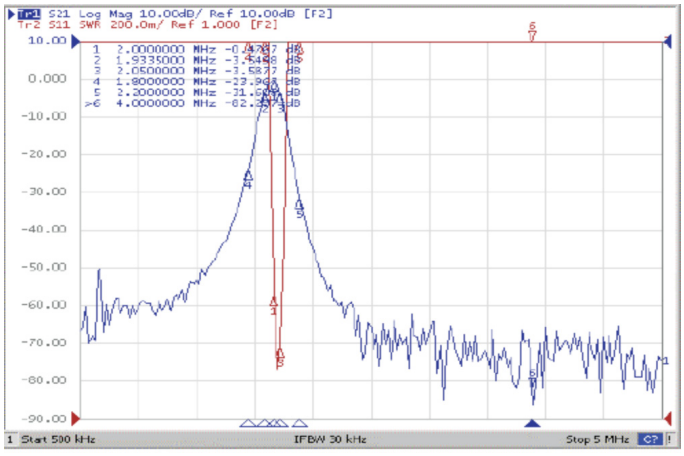

Figure 3. Frequency response of the narrowband tracking filter.

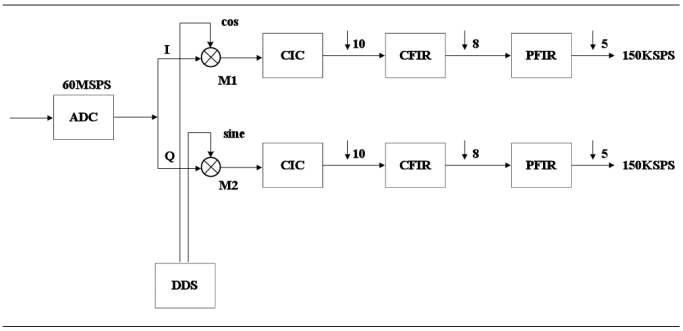

Figure 4. Block diagram of the DDC in the receiving path.

electromagnetic environment of the ionosonde station is better and the receiving antenna is large enough, then the preprocessor unit will be an optional component. Since the narrowband tracking filter in the preprocessor unit is an optional component to the whole system, an anti-aliasing filter is required before the stage of the ADC.

The output of the preprocessor unit is first fed to the stage of the AGC through the RF cable, and the AGC adjusts the amplitude of the signal in real-time to ensure that the analog signal through the anti-aliasing filter is in the range of the ADC. For the CAS-DIS, the AGC is implemented by a digitally controlled, variable-gain amplifier, with a gain and attenuation range from 30 dB to -12 dB. If the input amplitude of the ADC is large enough, the gain of the amplifier will become low under the control of the digital signal.

From a system point of view, the number of bits of the ADC is an important parameter for the performance of the receiver [Tsui 2004]. For the CAS-DIS, a high-performance ADC is used, where the ADC is 14-bit, and the full-scale analog input range is 2Vp-p. The test results show that the sensitivity of the digital receiver is -120 dBm at 150 kHz, and the instantaneous dynamic range is more than 80 dB, without taking the AGC into account.

For the CAS-DIS, the sampling rate of the ADC is 60 MHz. Because of the higher sampling rate, a process of the DDC is applied before the pulse compression processing. The four parts of the DDC are the digital mixers (M1, M2), the cascaded integrator-comb filter (CIC), the compensation filter (CFIR), and the programmable filter (PFIR). The clock of the DDC is equal to the sampling rate of the ADC, which is 60 MHz. The input signals of the M1 and M2 digital mixers are the digital signal of the ADC and the sine and cosine signals generated by the DDS. The outputs of the digital mixing from M1 and M2 are fed to the stage of the CIC. As the decimation rate of the CIC is 10, the sampling rate of the CIC output is 6 MHz. To compensate for the attenuation of the signal amplitude in the effective signal bandwidth caused by the stage of the CIC, two 29-order CFIRs are added after the stage of the CIC; the decimation rate of the CFIRs is 8, so the sampling rate after the CFIRs is 750 kHz. To further reduce the data rate, the final stages of the DDC are the PFIRs, which are two 128-order programmable FIR low-pass filters; the decimation rate of the PFIRs is 5. Therefore, the whole decimation rate of the DDC is 400, the output data rate of the DDC is 150 kHz, and the effective bandwidth of the output is limited within the range of 75 kHz. The two channels in Figure 4 are the I and Q channels of the DDC. Figure 5 shows the frequency response of the filters in the DDC, where the solid line in blue is the frequency response of the 5-order CIC filter. Taking into account the quantization noise, the suppression to the first sidelobe is more than 60 dB. The solid lines in green and red in Figure 5 are the frequency responses of CIC+CFIR and CIC+CFIR+PFIR, respectively.

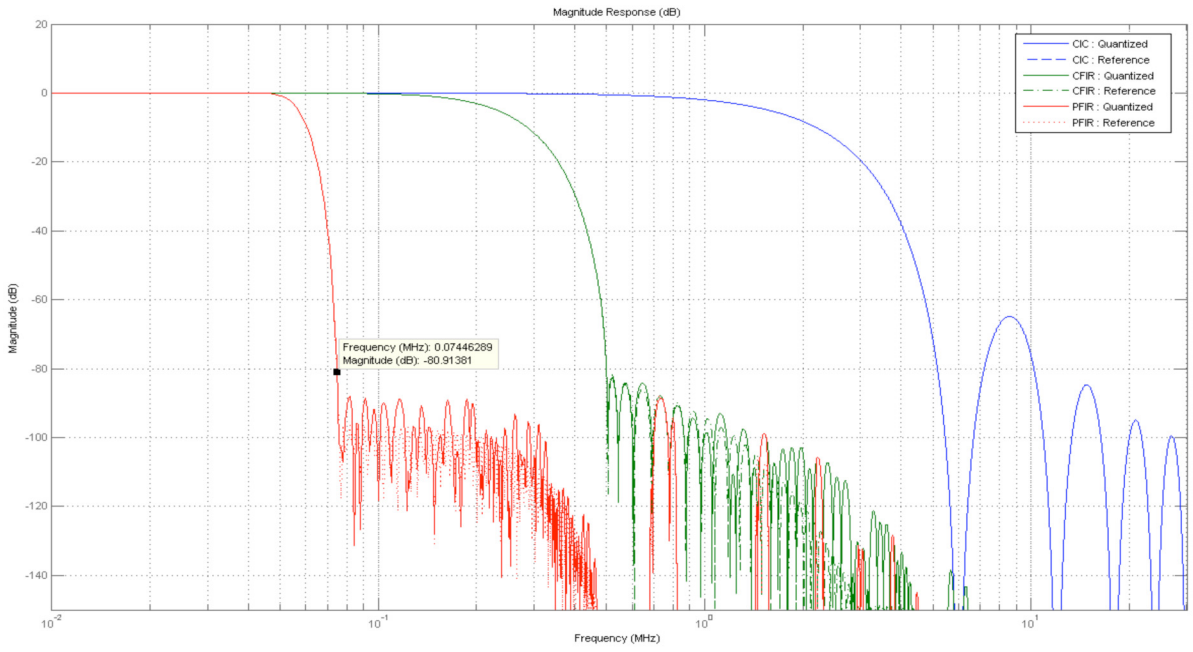

Figure 5. Frequency response of the CIC, CFIR and PFIR filters.

As discussed above, the ADC is sampling over about 6.0 ms in each PRF with the sampling rate of 60 MHz, so the total number of digital samples in each PRF is 360,000. As the decimation rate of the DDC is 400, a frame of data after the DDC in each PRF is 900 points, which corresponds to the detection range of 90 km to 990 km, and a synthetic detection precision of 1 km. For the CAS-DIS, the data of the I and Q components are 32-bit, which greatly improves the dynamic range of the receiver. The I and Q components are stored in one first-in, first-out unit after the coherent integration processing. When the records in the first-in, first-out unit reach 900, a direct memory interrupt occurs, and the I and Q components are sent to the PC through the peripheral component interconnect interface.

To improve the SNR of the echo signals, the technique of coherent pulse integration is used for the CAS-DIS. If two echoes are coherent, as they have the same phase they can be added together. The coherent integration of N signals can provide a factor of N improvement to the SNR [Cabrera et al. 2010]. If the N echoes are exactly coherent, then performing the integration on N echoes is equivalent to adding these echoes together, which yields an amplitude that is N times greater. As the noise of the received signal has a random phase, eventually the power of the echoes increases by a factor of N^2, while the power of the noise increases by a factor of N, and the improvement in the SNR is about $G = 20 \log\sqrt{N}(dB)$.

In actual fact, due to the instabilities of the system and the intrinsic variations that occur in the reflecting ionospheric layers, the echoes will lose coherence after a short time of integration. For the CAS-DIS, the maximum number of the integration is 128, which can provide an improvement of more than 20 dB to the SNR of the received signal. As shown in Figure 1, the unit of the coherent integration processor is part of the digital receiver, which is also implemented in the FPGA.

2.5. Pulse compression processing

Digital pulse compression techniques are routinely used for matched filtering, which can be divided into time-domain digital pulse compression and frequency-domain digital pulse compression. As the time-domain pulse compression is computationally intensive, frequency-domain digital pulse compression is used for the CAS-DIS. One of the input signals is the sampled sequence formed by the I and Q data from the DDC, and the other input signal is the replica of the reference waveforms filled with zeros. The process of pulse compression is performed on the PC. Three steps are included in the process of digital pulse compression: (1) taking the fast Fourier transform (FFT) of the sampled sequence; (2) multiplying the frequency-domain sequence of the sampled signal by the FFT of the replica of the reference waveforms; and (3) performing the inverse FFT of the composite frequency-domain sequence, to generate the time-domain compressed pulse. Figure 6 illustrates this process of digital pulse compression.

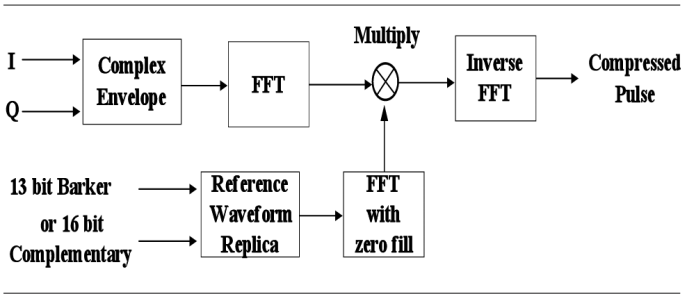

Figure 6. Block diagram of the digital pulse compression.

As the sampling time of the ADC is 6 ms, the output data rate of the DDC is 150 kSPS, and thus the total number of samples N in the PRF is 900. For improved implementation of the FFT, N is extended to the next power of two by zero padding. For some positive integer m, $N_{FFT} = 2^m \geqslant N$, so the length of FFT was chosen as 1024.

Figure 7 shows an example of baseband waves of I and Q data that were generated by the DDC with 100× phase coherent integration. Figure 8 shows the result after the pulse compression processing, where the blue and red lines are the pulse compression results of code A and code B of the 16-bit complementary code, and the cyan line is the added result of the two codes, from which it can be seen that an improve-

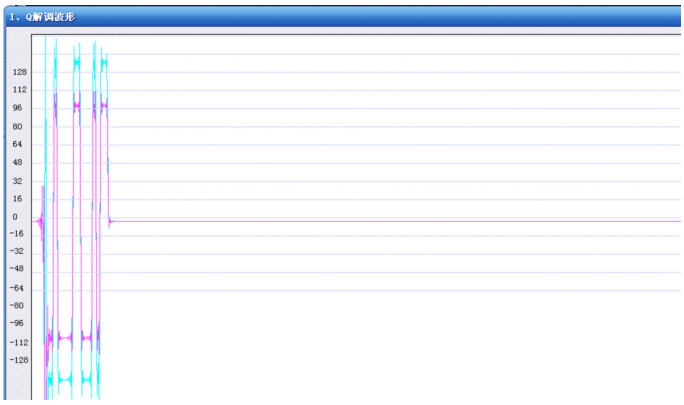

Figure 7. Baseband waves of the I and Q data after the DDC.

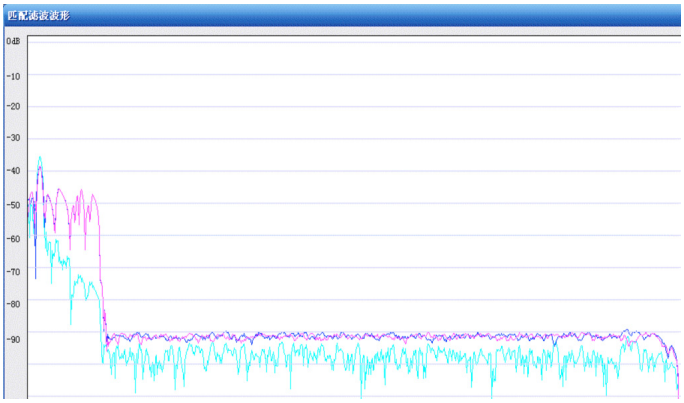

Figure 8. Result of the digital pulse compression processing.

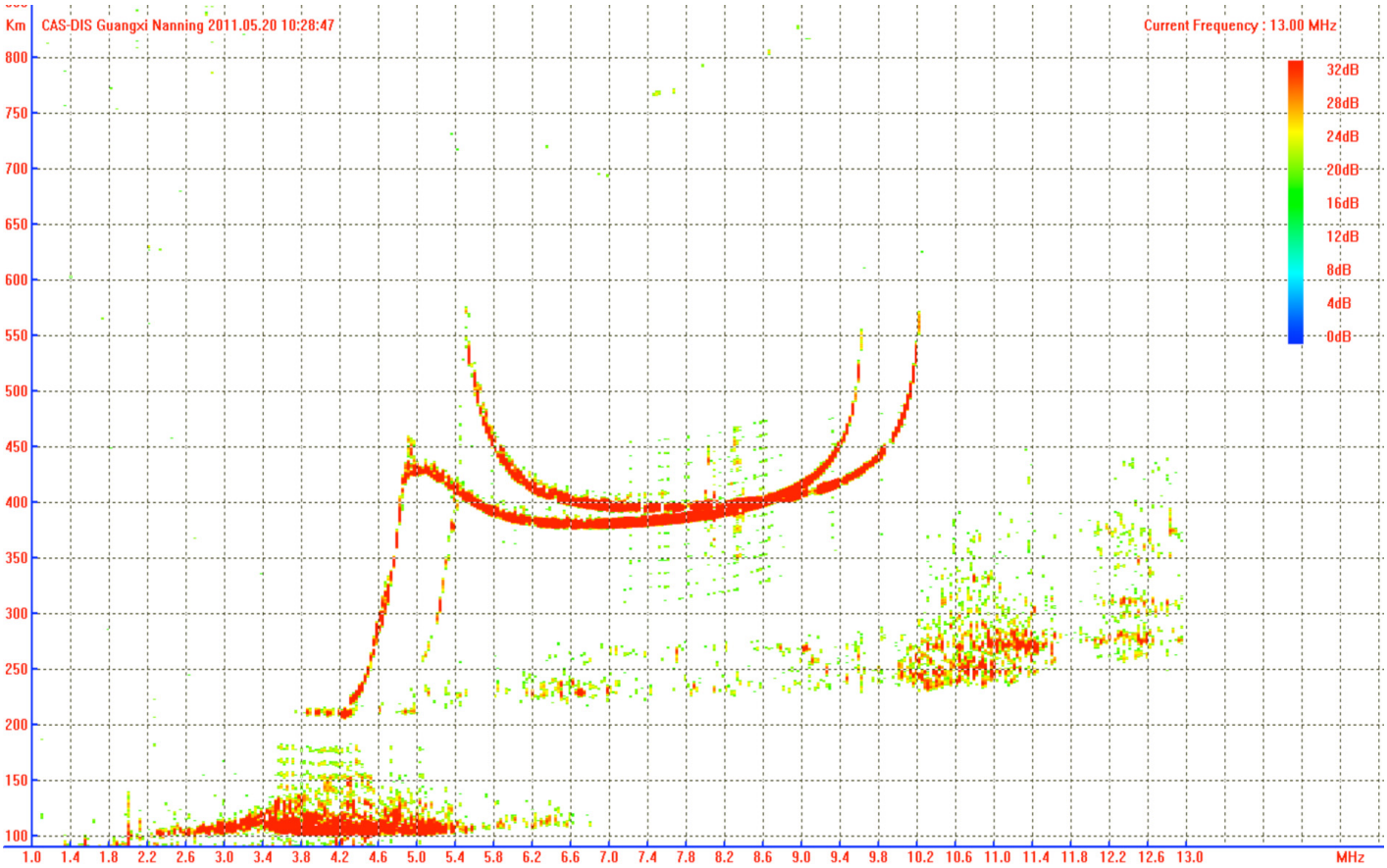

Figure 9. Test result of the CAS-DIS on May 20, 2011, for the Guangxi Nanning station (13-bit Barker code).

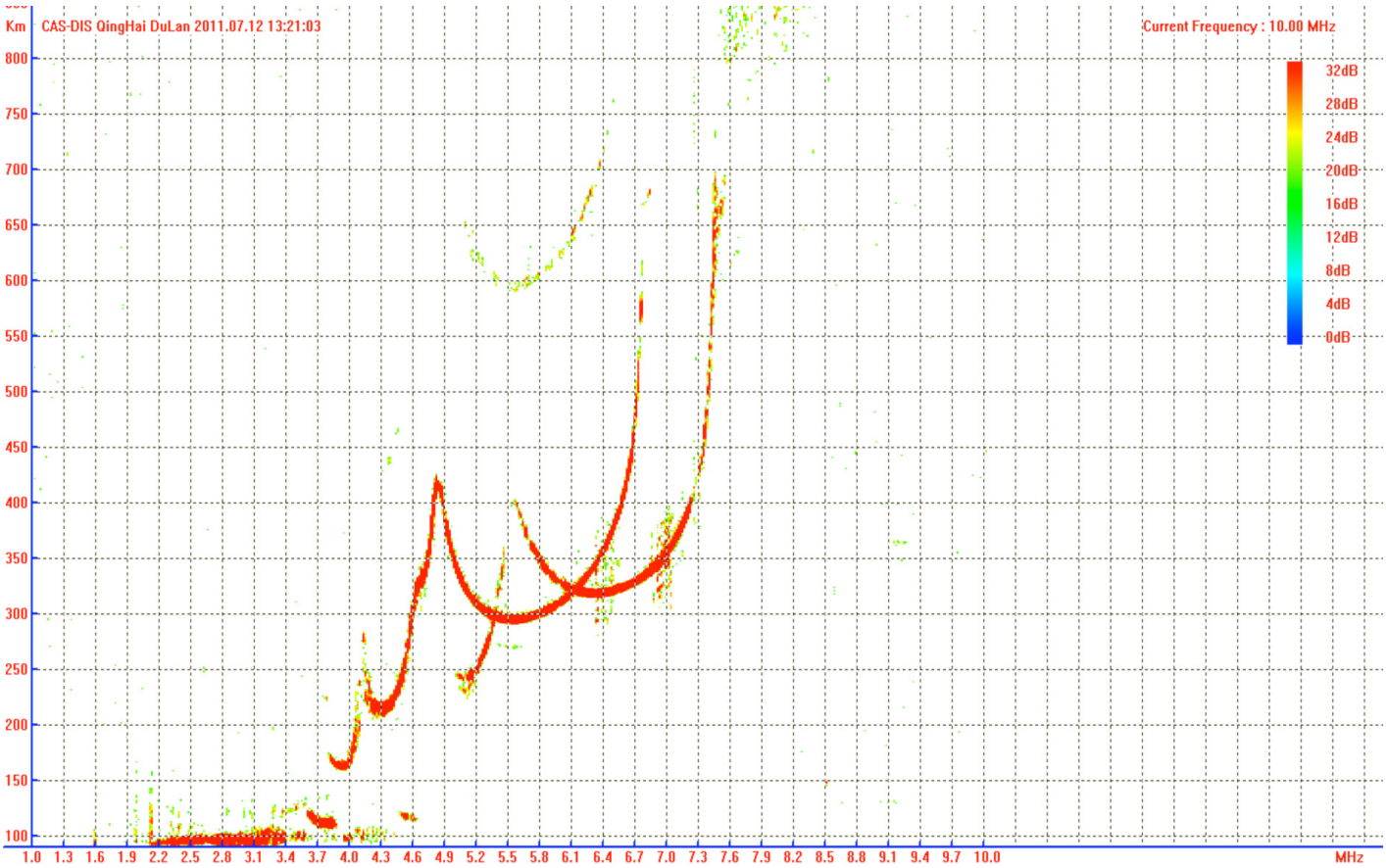

Figure 10. Test result of the CAS-DIS on July 12, 2011, for the Qinghai Dulan station (16-bit complementary code).

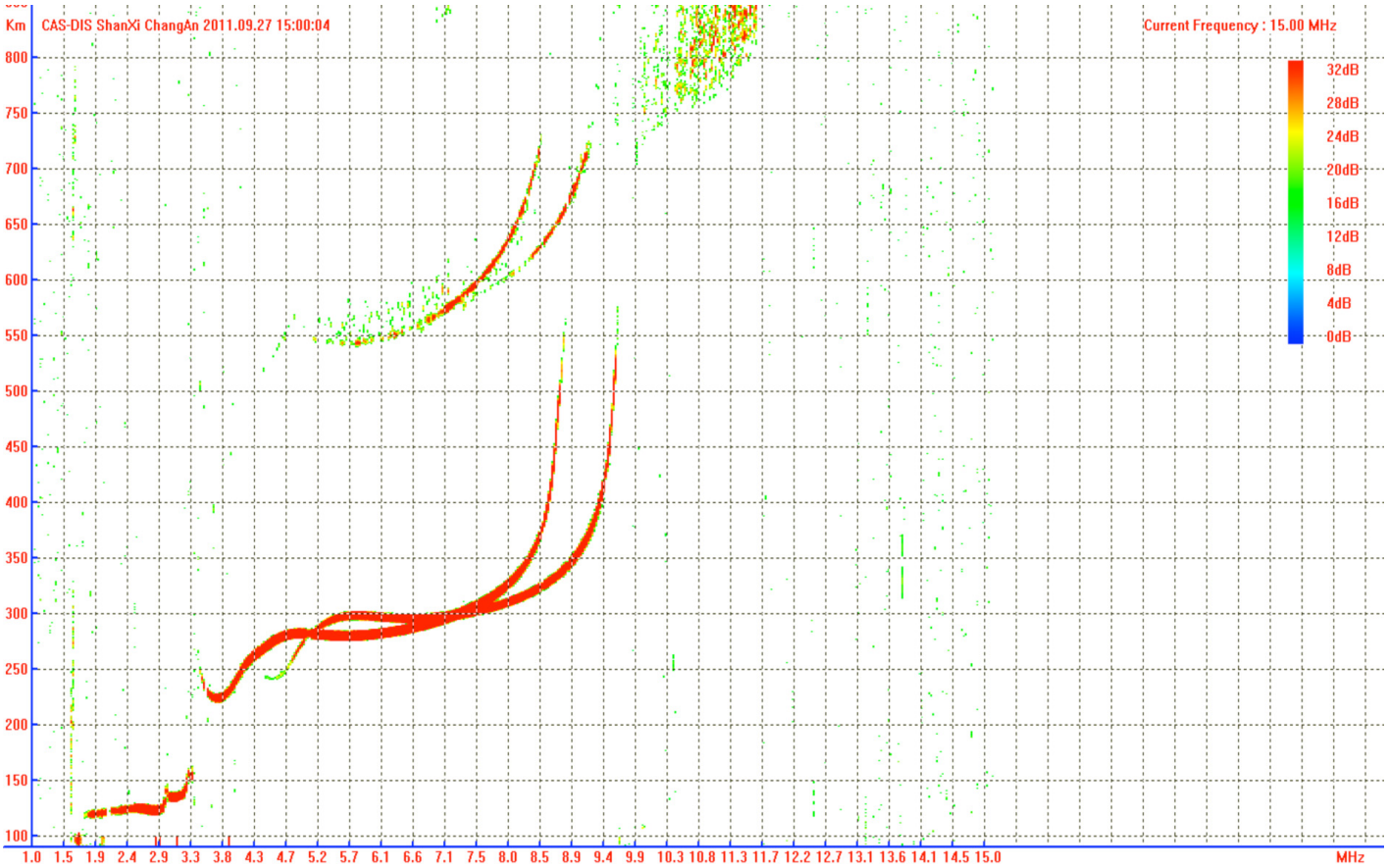

Figure 11. Test result of the CAS-DIS on Septemper 27, 2011, for the Shanxi Chang'an station (16-bit complementary code).

ment of more than 55 dB in the SNR can be achieved. Without taking account of any improvement by coherent integration with 20 dB, the SNR improvement of the 16-bit complementary code is about 35 dB. Although we do not show any examples for the 13-bit Barker code, the test results show that the improvement of the SNR using the 13-bit Barker code is about 22 dB.

2.6. Antenna system

For the CAS-DIS, both the transmitting and receiving antennas are delta antennas. The 600 ohm loads are installed on the top of the tower, and each has a balun that is used to match the balanced antennas with the unbalanced coaxial RF cable.

To obtain an improved performance, a simulation was performed before the antenna was implemented. These simulation results showed that the voltage standing-wave ratio and radiation efficiency of the delta antenna in a parallel two-line structure were significantly better than a single-line structure antenna. This will also improve with an increase in the dimension of the antenna, especially at lower frequencies. Therefore, the antenna is designed to use the parallel two-line structure, and the dimension is as large as possible, to improve the performance for the lower frequency of the system. Taking into account the performance and difficulty in the implementing of the large antenna, for the CAS-DIS the transmitting antenna uses the parallel two-line structure. This is approximately 30 m in height. The receiving antenna uses a single-line structure, which is about 25 m in height.

3. System performance and conclusions

3.1. Test results

The CAS-DIS was tested over a long period during 2011, with the production of a lot of high-quality ionograms; some of these results are presented here. In the ionograms, the horizontal axes show the frequencies in MHz, while the units of the vertical axes are km. In addition, the power scale in the top right-hand corner of the ionograms is a relative value, and the reference value is a coefficient times the average power of the echoes in each PRF.

Figure 9 shows an example of the ionogram produced by the CAS-DIS on May 20, 2011, at the Guangxi Nanning station, with the system working in 13-bit Barker code mode. Figures 10 and 11 show two more examples of ionograms produced by the CAS-DIS, on July 12, 2011, and September 27, 2011, at the Qinghai Dulan and Shanxi Chang'an stations, respectively. In these cases, the CAS-DIS worked in 16-bit complementary code mode. The test results show that echoes appear first from the lower E region, and subsequently, with a greater time delay, from the F1 and F2 regions. If the power of the reflected signals is large enough, then multiple reflections appear in the ionograms.

3.2. Conclusions

In this report, we have introduced a new ionosonde system, the CAS-DIS, in which the following key techniques are used:

– An FPGA device is used to define a digital receiver, and the echoed down-converted signals in discrete time domains (I and Q) are post-processed in the frequency domain, performing the FFT on the PC. The technological design is an attractive and simple conceptual method.

– The down-converter integrated-circuit chips are used to implement the function of the DDC in existing ionosonde systems. The output of these chips is less than 16-bit, which limits the dynamic range of the receiver. For the CAS-DIS, the implementation of the DDC is based on an FPGA platform and the output of the I and Q data are 32-bit, which enhances the dynamic range of the receiver.

– Phase encoding and digital pulse compression techniques: there are two kinds of code that can be selected in the CAS-DIS. The gain of the pulse compression process is about 22 dB in the 13-bit Barker code mode, while it can reach about 35 dB in the 16-bit complementary code mode, which depends on the noise level of the system.

– A phase coherent integration technique is used in the design of the CAS-DIS. The number of integrations is selectable from between 1 to 128, which provides more than a 20 dB gain in the SNR.

– A single ADC is used to digitize the received RF signal, and digital signal processing is used to perform the down-conversion to the I and Q baseband signals. To solve the problem of large instantaneous bandwidth in the digital receiver, a narrowband tracking filter is used. The center frequency of the filter tracks the carrier frequency in real-time, to ensure that the frequency components are filtered out of the effective bandwidth, which improves the performance of the system.

References

Bianchi, C., U. Sciacca, A. Zirizzotti, E. Zuchheretti and J.A. Baskaradas (2003). Signal processing techniques for phase-coded HF-VHF radars, Annals of Geophysics, 46 (4), 697-705.

Bibl, K. (1998). Evolution of the ionosonde, Annals of Geophysics, 41 (5/6), 667-680.

Cabrera, M.A., E. Zuccheretti, R.G. Ezquer, U. Sciacca, J.M. Lopez, M.G. Molina, J.A. Baskaradas (2010). Some considerations for different time domain signal processing in pulse compression radars, Annals of Geophysics, 53 (5/6), 1-11.

Mahafza, B.R. (2000). Radar system analysis and design using Matlab, Chapman & Hall, CRC, 263 pp.

Reinisch, B.W., et al. (2009). New Digisonde for research and monitoring applications, Radio Sci., 44, 1-15.

Tsui, J.B. (2004). Digital techniques for wideband receivers, SciTech Publishing Inc., 219 pp.

Zuccheretti, E., G. Tutone, U. Sciacca, C. Bianchi and J.A. Baskaradas (2003). The new AIS-INGV digital ionosonde, Annals of Geophysics, 46 (4), 647-659.

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