ACTA IMEKO
ISSN: 2221-870X
December 2016, Volume 5, Number 4, 29-36

Enhancement of flash memory endurance using short pulsed program/erase signals

Philippe Chiquet[1], Jérémy Postel-Pellerin[1], Célia Tuninetti[2], Sarra Souiki-Figuigui[1], Pascal Masson[2]

[1]*Aix-Marseille Universite, IM2NP-CNRS UMR 7334, rue Frederic Joliot-Curie, 13451 Marseille, France*
[2]*Nice Sophia-Antipolis University EPOC, 06410 Biot, France*

ABSTRACT
The present paper proposes to investigate the effect of short pulsed Program/Erase signals on the functioning of Flash memory transistors. Usually, electrical operations related to said devices involve the application of single long pulses to various terminals of the transistor to induce various tunneling effects allowing the variation of the floating gate charge. According to the literature, the oxide degradation occurring after a number of electrical operations, leading to loss of performance and reliability, can be reduced by replacing DC stress by AC stress or by reducing the time spent under polarization by the MOS-based devices. After a brief presentation of the functioning of the Flash memory transistors tested in this work, the experimental setup used to replace standard electric signals with short pulses will be described. Electrical results showing the benefits of programming and erasing non-volatile memories with short pulses will then be presented.

Section: RESEARCH PAPER

Keywords: Non-Volatile Memory; Flash; reliability; advanced electrical characterization

Citation: Philippe Chiquet, Jérémy Postel-Pellerin, Célia Tuninetti, Sarra Souiki-Figuigui, Pascal Masson, Enhancement of flash memory endurance using short pulsed program/erase signals, Acta IMEKO, vol. 5, no. 4, article 6, December 2016, identifier: IMEKO-ACTA-05 (2016)-04-06

Section Editor: Lorenzo Ciani, University of Florence, Italy

Received September 26, 2016; **In final form** November 6, 2016; **Published** December 2016

Corresponding author: Philippe Chiquet, e-mail: philippe.chiquet@im2np.fr

1. INTRODUCTION

Over the last few years, Flash memory cells, which can nowadays be found in common products such as USB flash drives and smart cards, have become the dominant non-volatile memory devices in the semiconductor industry. Flash memory is built around a floating gate transistor, a MOS transistor to which an extra tri-layer stack oxide "Oxide/Nitride/Oxide" (ONO) and a top electrode (control gate) have been added, as shown in Figure 1. Information is stored in the device as an electric charge located in the floating gate which, thanks to the various oxide layers surrounding it, retains this charge when the power supply is removed, thus assuring the non-volatile behaviour of the Flash transistor [1].

According to the value Q_{FG} of this charge, two distinct logical states '0' and '1' can be differentiated, and the threshold voltage V_T of the transistor can be calculated according to equation (1):

$$V_T = V_{T0} - \frac{Q_{FG}}{C_{PP}}, \quad (1)$$

where V_{T0} is the natural threshold voltage of the cell and C_{PP} the control gate / ONO / floating gate capacitance [2].

The transition from one state to the other is obtained when electric signals are applied to some of the transistor's terminals, inducing the injection (or removal) of electrons into (or from) the floating gate through the tunnel oxide. In the remainder of this paper, the logical states corresponding to the highest and lowest threshold voltage values of the floating gate transistor will be called the "programmed" and "erased" states

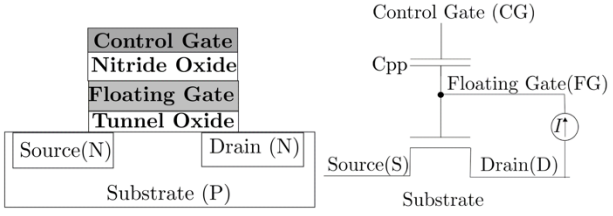

Figure 1. Schematic (left) and electric (right) representation of a Flash floating-gate transistor.

respectively. Programming is usually achieved through Channel Hot Electron (CHE) injection in Flash memories, while erasing is generally obtained thanks to Fowler-Nordheim (FN) injection [3].

Due to this functioning, the tunnel oxide layer, which can be degraded due to repeated electrical operations, is critical to the reliability of the memory devices and various solutions can be considered in order to improve their overall reliability [4]. The present work will focus on the use of short-pulsed signals, which consists in replacing long standard signals by a series of pulses with short plateau widths, as previous studies show that MOS-based devices are less impacted by AC stress than DC stress [5]-[11], or by shorter pulses of higher amplitude [12].

2. GENERATION OF SHORT-PULSED SIGNALS

2.1. Experimental setup

In order to investigate the endurance of the tested Flash memory cells under short pulses, a complete setup has been developed with the help of a Keysight Semiconductor Device Parameter Analyzer B1500A [13] equipped with two WGFMUs (Waveform Generator Fast Measurement Unit B1530A), two SPGUs (Semiconductor Pulse Generator Unit) and four SMUs (Source Monitor Unit), as described in Figure 2. The SMUs are used to measure the $I_{DS}(V_{GS})$ characteristics necessary to the reading (threshold voltage extraction at a given drain current value) of the cell state while the SPGU enables the definition of pulses for the successive programming/erasing operations. An Agilent 16440A selector switches between the SMU and SPGU during the endurance test. The additional WGFMU in the setup, connected via RSU (Remote-Sense and Switch Unit) enables the definition of arbitrary waveforms and the dynamic measurement of the drain current, which can be useful when evaluating the consumption of the programming operation during the endurance test [14], [15].

2.2. Definition of the applied signals

Standard (STD) Flash CHE signals consist in simultaneous control gate and drain pulses of amplitude V_{PP} equal to +9 V (during 5 µs) and +4.2 V (during 1 µs) respectively, while standard FN erasing is obtained by applying a single 500 µs pulse of amplitude V_{PP} equal to −18 V on the control gate.

The first approach here, which will be developed in Section 3, consists in replacing standard programming and/or erasing signals by trains of short pulses. These new signals have been chosen so as the "programmed" and "erased" threshold voltages measured for a fresh Flash device are close to the threshold voltage values obtained when standard signals are used. It has been experimentally observed that such a condition is met when the total plateau time spent on short pulses is equal to the duration of the standard signal. In order to obtain comparable threshold values using series of short pulses, the standard drain signal in CHE programming and the standard control gate signal in FN erasing have respectively been transformed into a series of 20 pulses of 50 ns plateau time and a series of 10,000 pulses of 50 ns plateau time. In each case, the signals created with the experimental setup described above have been checked with the help of an oscilloscope as seen in Figures 3 to 5.

The second approach, which will be the topic of section 4, is much simpler on an experimental level and consists in replacing standard signals with single pulses of higher amplitude and shorter plateau time.

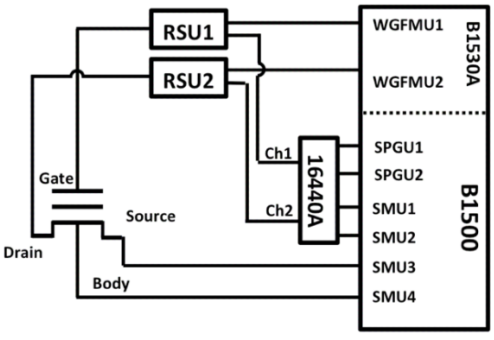

Figure 2. Experimental setup used to perform endurance tests with current consumption measurements.

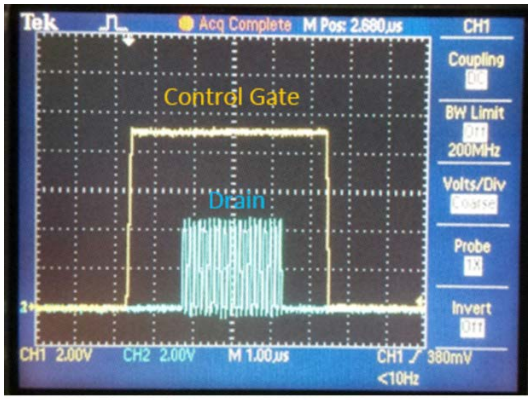

Figure 3. Oscilloscope observation of the control gate (yellow) and drain (blue) signals for a short-pulsed CHE programming of the Flash memory cells.

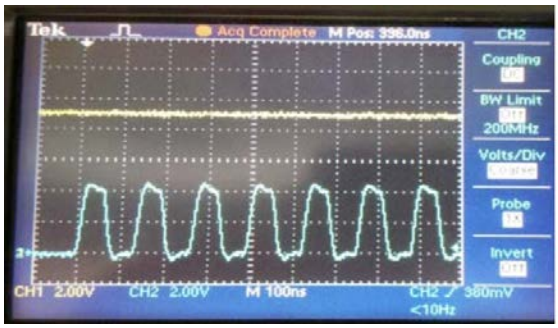

Figure 4. Close-up observation of signals observed in Figure 3.

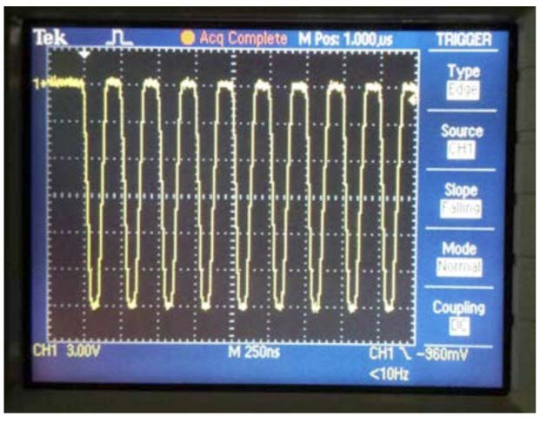

Figure 5. Oscilloscope observation of the control gate signal of a Flash floating gate transistor during a FN erase operation.

3. ELECTRICAL RESULTS: PULSE TRAINS

3.1. Qualitative results and total window closure

Measurements carried out on numerous devices yielded electrical results highlighting the effect of pulsed program/erase operations on Flash memory endurance. Endurance of memory cells is mainly characterized by the evolution of their programming window, defined as the difference between the threshold voltages of the "programmed" and "erased" states, over numerous program/erase electrical operations.

In order to quantify the gradual programming window closure linked to device degradation, a criterion had to be chosen. In the present work, the total window closure ΔV_T after k program/erase cycles, defined by equations (2) and (3) has been retained:

$$\Delta V_T = \Delta V_T^{prog} - \Delta V_T^{erase}, \quad (2)$$

$$\Delta V_T^{prog,erase}(k) = V_T^{prog,erase}(k) - V_T^{prog,erase}(1). \quad (3)$$

According to its definition, ΔV_T is calculated as the sum of two negative values and represents the combined shifts of the "programmed" and "erased" threshold voltages. This total window closure is plotted in Figure 6 as a function of the number of program/erase cycles up to 10^6 cycles. It can be seen that both the Short (20×50 ns)/STD and STD/Short (10000×50 ns) cyclings provide a decrease in programming window closure of about 0.5 V compared to the STD/STD cycling.

In order to understand the effect of the pulses' parameters on this observed endurance improvement, measurements involving different plateau amplitudes and duty cycles have been carried out.

3.2. Effect of pulse amplitude

Electrical results presented in Figure 7 compare the programming window closure of the STD/Short (10000×50 ns) and STD/STD cyclings for V_{PP} values of −17 V, −18 V and −19 V. While a difference in programming window closure between the two cycling modes can be observed for the first two V_{PP} values after 10^4 cycles, erasing at V_{PP} = −19 V with short pulses instead of the standard signal makes no difference. This could be explained by the fact that at a given duty cycle, the benefits of replacing DC stress with AC stress become noticeable only if the plateau time of the pulses is reduced as much as possible as the stressing field is increased [11]. Other studies have also shown that such results cannot be achieved at ambient temperature when plateau times of the applied pulses become long enough [5].

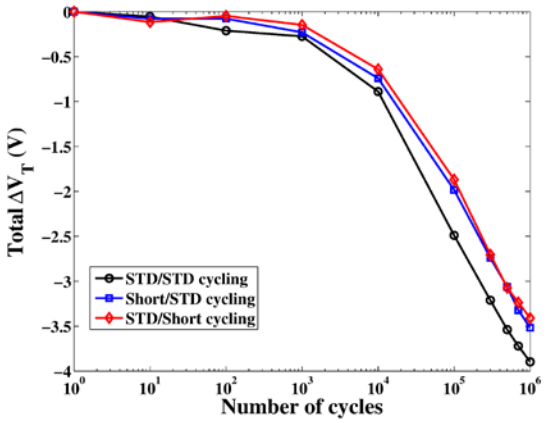

Figure 6. Programming window closure up to 10^6 program/erase (STD/STD, Short/STD and STD/Short) cycles. Each measurement point has been averaged over ten Flash memory cells.

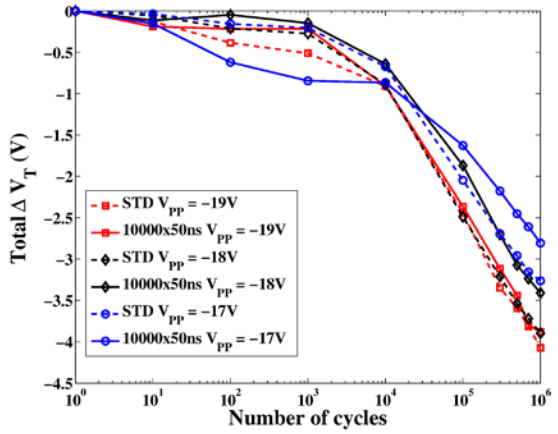

Figure 7. Programming window closure up to 10^6 program/erase (STD/STD and STD/Short) cycles for various erasing V_{PP} values. Each measurement point has been averaged over ten Flash memory cells.

3.3. Effect of duty cycle

In order to achieve lower device degradation, allowing oxide relaxation during electrical stress is a common solution [5], [16]. It has been achieved in this study by increasing the delay between the short pulses constituting the signals applied to the control gate and the drain of the transistor. The duty cycle, which is defined as the ratio of the plateau duration t_{pl} to the period value T as shown in Figure 8, is thus decreased.

Electrical results obtained after Short/Short cycling (V_{PP} = −18 V) for duty cycles equal to 0.1 and 0.01 have been compared to experimental data obtained for STD/STD cycling in Figure 9. It can be observed that decreasing the duty cycle allows to reduce the programming window closure. Using experimental data from Figure 9 allows to plot ΔV_T as a function of the duty cycle as shown in Figure 10. The total window closure is shown to have a logarithmic behaviour with respect to duty cycle.

3.4. Measurement of device consumption

Energy consumption of non-volatile memory devices has been of recent interest as experimental possibilities offered with the coming of new parameter analyzers in recent years [14], [15]. It can be defined according to the following equation (4):

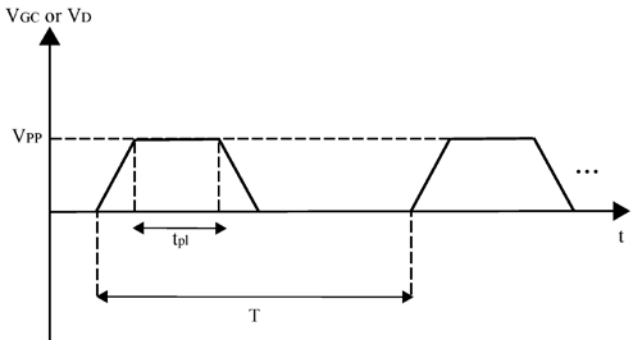

Figure 8. Schematic representation of a period of the electrical signals applied to the control gate (V_{GC}) or drain (V_D) of the memory transistor. The duty cycle is calculated as the ratio of the plateau duration t_{pl} to the period value T.

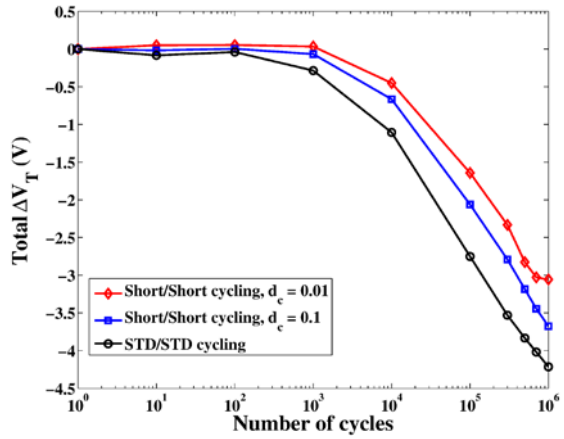

Figure 9. Programming window closure up to 10^6 program/erase cycles obtained for various duty cycle values. Each measurement point has been averaged over ten Flash memory cells.

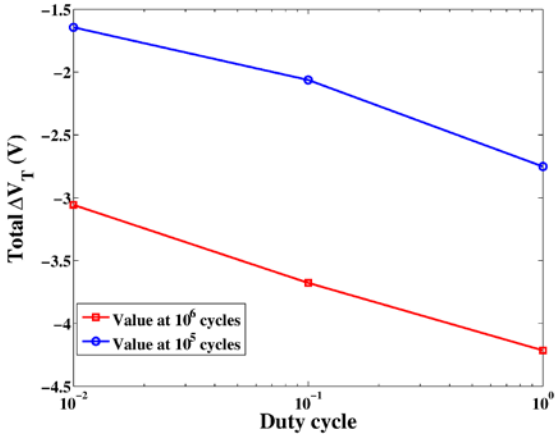

Figure 10. Total window closure as a function of duty cycle obtained from data of Figure 9 at 10^5 and 10^6 cycles.

$$E_C = \int V_{DS} I_{DS} dt \,, \tag{4}$$

where V_{DS} and I_{DS} are the drain-source voltage and the drain current of the transistor, respectively. Results of time-resolved measurements of drain current performed during a programming operation before and after electrical cycling (STD/STD and Short/STD), which can be observed in Figures 11 and 12, show that device consumption typically increases with device degradation.

Figure 13 allows a comparison between the respective consumptions of a fresh Flash device during STD and Short programming operations. Taking (4) into consideration, it is pretty obvious that device consumption is higher in the latter case, as the integral of the red curve (Short) is clearly higher than that of the black one (STD). It can be easily explained as in this case, the pulses constituting the Short programming signal are characterized by rise and fall times of the same order of magnitude as the plateau times. These rise and fall times, which do not exist during a STD programming signal, make up an important part of the Short signal and thus explain this consumption increase.

3.5. Reliability of Flash memory cells under various cycling modes

The statistical behaviour of Flash cell populations subjected to STD/STD, Short/Short (duty cycle equal to 0.1), and

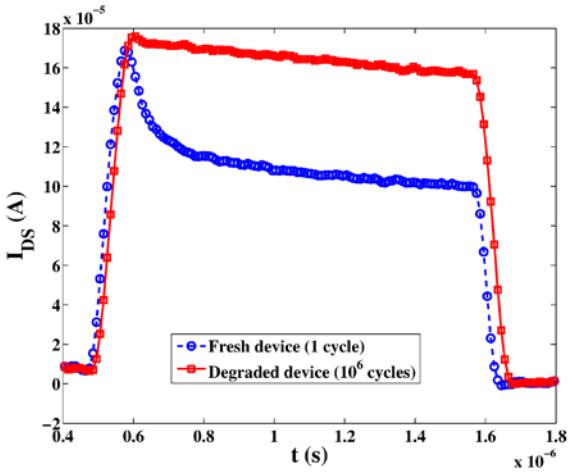

Figure 11. Time-resolved measurement of the drain current I_{DS} during a standard programming signal before (circles) and after (squares) STD/STD program/erase cycling (10^6 cycles).

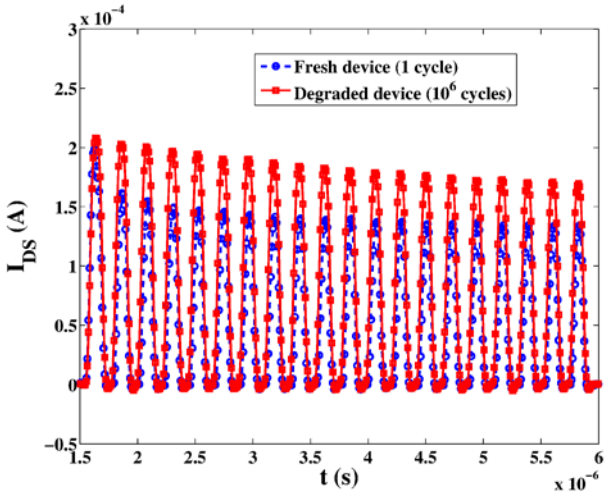

Figure 12. Time-resolved measurement of the drain current I_{DS} during a short (20x50 ns) programming signal before (circles) and after (squares) short/STD program/erase cycling (10^6 cycles).

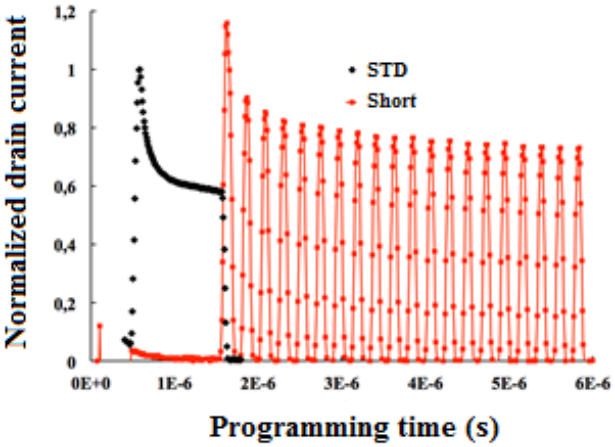

Figure 13. Current consumption measurements during STD (black) and Short (red) programming operations performed on a fresh Flash device.

STD/Short (V_{PP} = −17 V) cyclings has been investigated. Flash memory cells remain functional as long as their programming window remains greater than a certain value, below which the

two logical states cannot be distinguished anymore. In that case, the threshold voltage value obtained when reading such a cell would not allow determining if it is "programmed" or "erased". For each cycling mode, the cells were considered failed when the programming window went below 2 V.

Generally speaking, failure of electronic systems or components over time has often been described using a Weibull distribution [17], [18]. Assuming such a distribution in the present case, the ratio of failed cells after k program/erase cycles $F(k)$ can be written according to equation (5):

$$F(k) = 1 - e^{-\left(\frac{k-k_0}{\tau}\right)^{\beta}}, \quad (5)$$

where k_0, τ and β are three fitting parameters of the distribution. Weibull plots of experimental data obtained from the three cell populations are presented in Figure 14. It can be seen that the failure of the tested Flash memory cells can be well described by a Weibull distribution. The fitting of experimental data of the three cell populations is realized using the parameter values reported in Table 1. As expected, cycling Flash cells with signals that are less degrading induces a shift of the failed cell distribution towards higher numbers of cycles.

The failure rate [19]-[21] $\lambda(k)$ can be expressed as a function of the number of cells still functional after k cycles $N(k)$ according to equation (6):

$$\lambda(k) = -\frac{1}{N(k)}\frac{dN(k)}{dk}. \quad (6)$$

The "bathtub" shape of the failure rate, calculated from experimental data of the three cell populations and shown in Figure 15, is typical for such statistical distributions [18], [22].

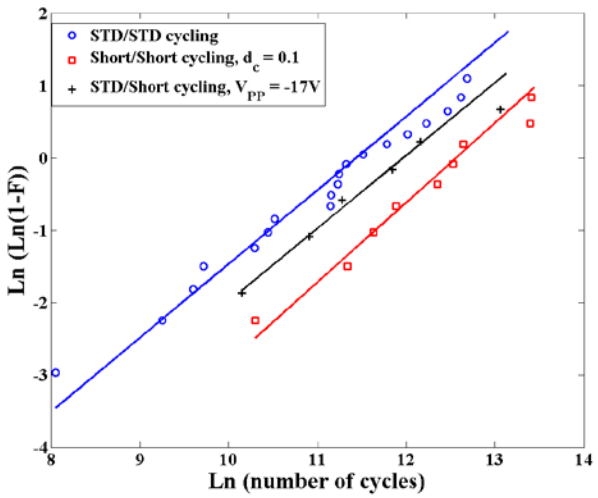

Figure 14. Weibull plot obtained for Flash memory cells subjected to STD/STD, Short/Short (dc = 0.1), and STD/Short (V_{PP} = -17 V) cyclings. The lines displayed in that figure correspond to the fitting of experimental data using Weibull parameters found in table Table 1.

Table 1. Best Weibull parameters allowing the fitting of experimental data for memory cells subjected to STD/STD, Short/Short (dc = 0.1), and STD/Short (V_{PP} = -17 V) cyclings.

Cycling Condition	k_0	τ	β
STD/STD	6.11×10^4	9.29×10^4	1.02
Short/Short d_c = 0.1	1.56×10^5	2.86×10^5	1.10
STD/Short Vpp=-17 V	5.78×10^4	1.58×10^5	1.01

4. ELECTRICAL RESULTS: SINGLE SHORT ERASE PULSE

While the last section investigates the consequences of changing standard program/erase signals into series of short pulses, the idea is here to find the electrical characteristics of a short single pulse that can be used to replace a given standard signal during device operation. The study presented in this section has been limited to erasing pulses.

4.1. Choice of the erase pulse characteristics

In order to achieve better electrical performance by speeding up the erasing process while targeting a similar V_T^{erase} value, the new pulse will be characterized by a shorter plateau time and a higher amplitude (i.e. t_{pl} < 500 µs and $|V_{PP}|$ > 18 V). Under these conditions, the necessary plateau time value for a given pulse amplitude can be determined by studying the erasing kinetics of the tested Flash devices, according to the method described in Figure 16. Successive short pulses are applied to the control gate of a programmed cell in order to obtain a progressive shift of its threshold voltage for a given V_{PP} value. The evolution of the threshold voltage can be monitored

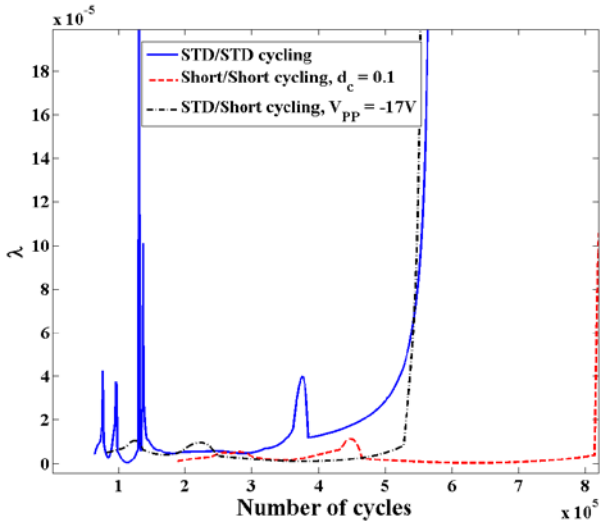

Figure 15. Calculated failure rate of Flash memory cells subjected to STD/STD, Short/Short (dc = 0.1), and STD/Short (V_{PP} = -17 V) cyclings.

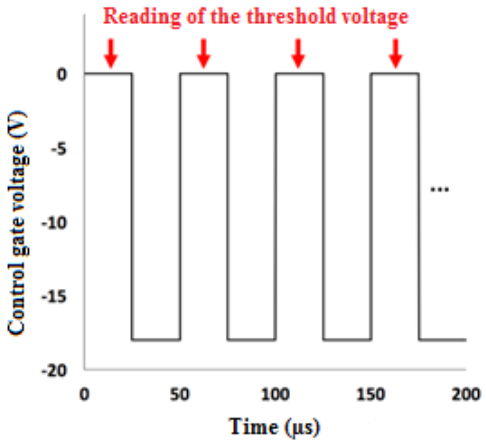

Figure 16. Experimental method to investigate erasing kinetics of the tested Flash cells.

through reading operations performed between these individual pulses.

Electrical results for V_{PP} values ranging from −18 V to −23 V and from −24 V to −31 V are displayed on Figures 17 and 18, respectively, where the threshold voltage evolution is plotted as a function of the erasing time, defined in this experiment as the total plateau time spent on the various pulses depicted in Figure 16. The particular erasing time needed to reach the targeted V_T^{erase} value (equal to 2.9 V as measured after an erasing operation using a standard signal) can be extracted for each V_{PP} value as the intersection point between the corresponding experimental curve and the dotted line in both figures.

These results show that for appropriate amplitudes (typically $|V_{PP}| > 26$ V), the erasing pulse's plateau time could be shorter than 50 ns to reach a V_T^{erase} value of 2.9 V. Assuming rise/fall times of 100 ns and t_{pl} = 50 ns, the standard erasing operation (lasting around 500 µs) could be sped up by a factor 2000, all the while retaining the typically low Fowler-Nordheim current consumption. The use of shorter and higher-amplitude erasing pulses could thus be considered for various applications where higher voltages are tolerated and higher device speed is of primordial importance.

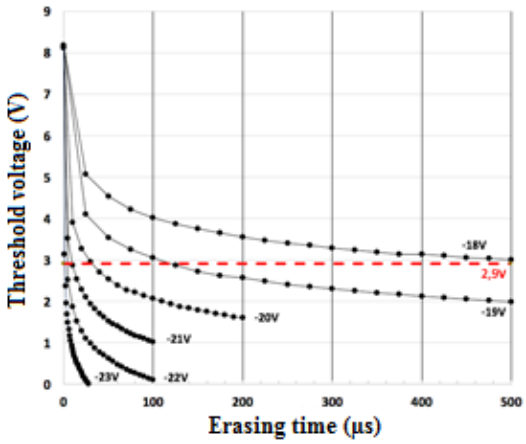

Figure 17. Erasing kinetics for -23 V < V_{PP} < -18 V. "Erased" threshold voltage measured after a standard erasing operation is added for comparison (dotted line).

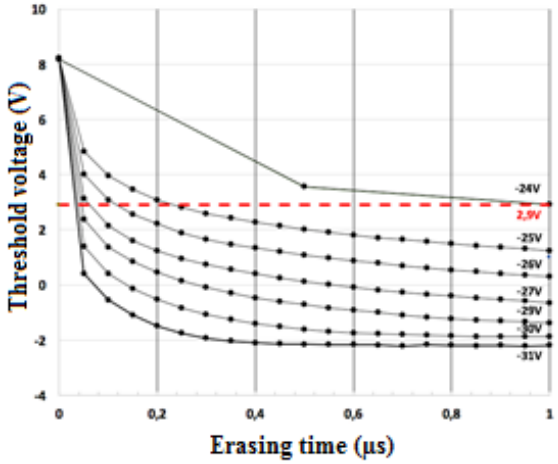

Figure 18. Erasing kinetics for -31 V < V_{PP} < -24 V. "Erased" threshold voltage measured after a standard erasing operation is added for comparison (dotted line).

4.2. Total window closure

In order to test the endurance of Flash cells subject to these new erasing pulses, electrical program/erase cyclings (with standard programming operations) have been performed for V_{PP} values ranging from −18 V to −28 V. Results presented in Figure 19 show that the total window closure of the Flash cells is decreased when compared to the STD/STD case (V_{PP} = −18 V). It can however be noticed that the Flash devices' endurance is optimal for an intermediate V_{PP} value which seems to be around −20 V.

Device degradation, monitored through programming window closure, should be more important as the amplitude of the erasing pulse increases (see Figure 7 for example), but that phenomenon is compensated by the resulting decrease of the plateau time. To further explain the existence of such an optimal amplitude value, TCAD simulations could be considered in order to monitor the temporal evolution of the tunnel oxide electric field in each case, and in particular, to try to estimate the impact of the erasing pulse rise time, which should limit the oxide electric field at higher V_{PP} values.

Endurance tests have also been performed for V_{PP} values up to −40 V, but due to technical limitations of the parameter analyzer used for this study (the minimum value that can be set for t_{pl} being 10 ns), the approach presented at the beginning of this section had to be modified. For erasing pulses of amplitude equal to −30 V, −35 V and −40 V plateau time had to be set to 10 ns, and as a consequence the obtained threshold voltages (reported in Table 2) are well below the standard value (i.e. 2.9 V). Electrical results presented in Figure 20 show that window closure is generally smaller than the one obtained with standard signals, except for V_{PP} = −40 V. Even in the latter case where the window closure is close to the standard one, it should not be as critical for device operation as the initial programming window is much larger to begin with.

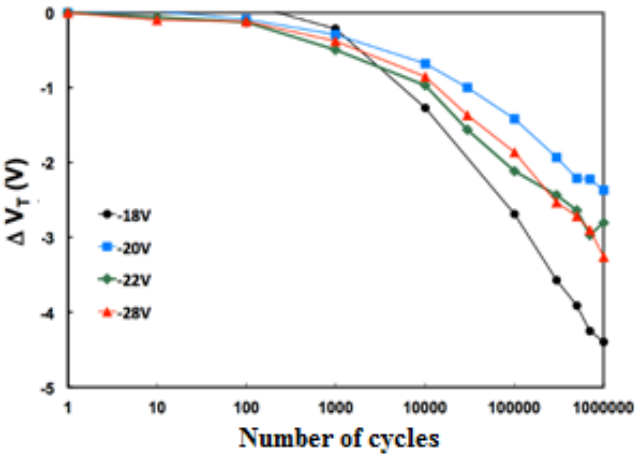

Figure 19. Programming window closure up to 10^6 program/erase cycles for various erasing V_{PP} values (from -18 V to -28 V). Each measurement point has been averaged over ten Flash memory cells.

Table 2. "Erased" V_T values obtained for t_{pl} = 10 ns.

Amplitude	Threshold voltage
-30 V	2 V
-35 V	-3 V
-40 V	-6.8 V

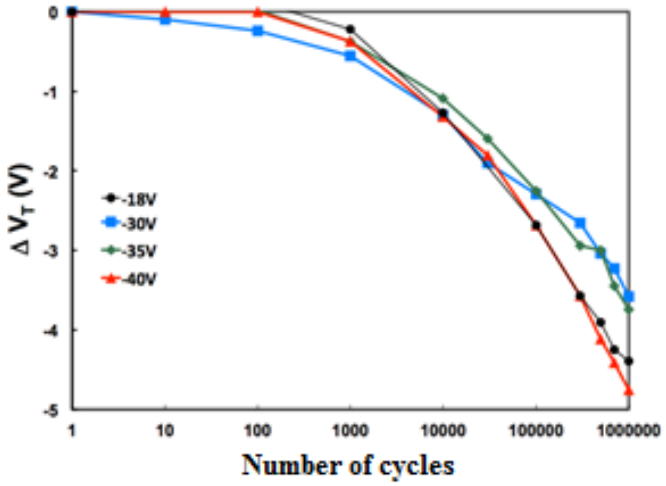

Figure 20. Programming window closure up to 10^6 program/erase cycles for various erasing V_{PP} values (from -30 V to -40 V, with standard -18 V results for comparison). Each measurement point has been averaged over ten Flash memory cells.

5. CONCLUSIONS

The impact of the use of short pulses on the endurance of Flash memories during the CHE programming and FN erasing operations has been investigated in this paper. The proposed experimental setup helped produce two main types of signals (trains of short pulses or single short pulses of high amplitude) that could potentially be used for specific industrial applications.

Replacing standard program/erase signals by trains of short pulses with plateau times as low as 50 ns allowed the observation of a decrease in programming window closure during program/erase cycling. The impact on this closure of parameters such as amplitude or duty cycle of the signals applied to the terminals of the memory transistors has been investigated. As the results presented in Section 3 show, the endurance improvement obtained by replacing standard control gate and drain signals by series of short pulses can only occur at a cost as the overall signal durations and device consumption have been shown to increase. This trade-off could prove useful in specific application fields (i.e. automotive and avionic industries) where reliability of the memory devices is the most important factor. Moreover, automotive and avionic applications typically require memory devices to operate within a much larger temperature range (typically −40 °C to 150 °C). As some other authors have shown, decreasing the duty cycle value yields better electrical results at higher temperatures [5], making the present results potentially even more interesting for such applications.

Replacing standard (erasing) signals by single shorter pulses of higher amplitude seems to be another recipe to produce a noticeable enhancement of the endurance of Flash memory devices, as the programming window closure has also been shown to decrease in this case. Moreover, current consumption should remain quite low, and the erasing speed can potentially be greatly improved. On the downside, these signals should only be used for applications in which higher voltages can be tolerated.

As a perspective, many other types of measurements could be considered to complete the study presented here. Firstly, both approaches showcased respectively in Sections 3 and 4 of this paper could probably be combined to maximize the endurance enhancement of Flash devices (i.e. train of short pulses characterized by $|V_{PP}| > 18$ V). Moreover, measurements presented in this work could be reproduced using different plateau times, duty cycles, rise/fall times to be able to understand the effect of these parameters on device degradation and to optimize them. Finally, complementary measurements could be performed on test MOS capacitors to investigate the effect of short-pulsed electrical stress in terms of interface trap density [16] and stress induced leakage current (SILC), which are physical manifestations of oxide degradation that can lead to program/erase window closure in non-volatile memory devices.

ACKNOWLEDGEMENT

Authors wish to thank Jean-Luc Ogier (STMicroelectronics, Rousset) for his technical support.

REFERENCES

[1] W.Brown, J.Brewer, "Nonvolatile semiconductor memory technology: a comprehensive guide to understanding and to using NVSM devices", IEEE Press, 1998.

[2] P. Pavan, R. Bez, P. Olivo, E. Zanoni, "Flash memory cells - an overview", Proc. of the IEEE 85 (8) (1999), pp. 1248-1271.

[3] R.Laffont, R.Bouchakour, O.Pizzuto, J.-M.Mirabel, "A 0.18 um flash source side erasing improvement", Proceedings of NVMTS (2004), pp. 105-109.

[4] J.Postel-Pellerin, G.Micolau, P.Chiquet, J.Melkonian, G.Just, D.Boyer, C.Ginoux, "Setting up of a floating gate test bench in a low noise environment to measure very low tunnelling currents", Acta Imeko, vol.4, No.3, 2015, pp. 36-41.

[5] B.Rebuffat, J-L.Ogier, P.Masson, M.Mantelli, R.Laffont, "Relaxation Effect on cycling on NOR Flash memories", Proc. of IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), 2015, pp. 613-616.

[6] A.Cester, A.Paccagnella, G.Ghidini, "Stress induced leakage current under pulsed voltage stress", Solid-State Electronics, vol.46, 2002, pp. 399-405.

[7] M.Nafria, J.Sune, D.Yelamos, X.Aymerich, "High field dynamic stress of thin SiO2 films", Microelectron. Reliab., vol.35, No.3, 1995, pp. 539-553.

[8] D.Caputo, R.Feruglio, F.Irrera, B.Ricco "Effect of pulsed stress on leakage current in MOS capacitors for non-volatile memory applications", Proc. of IEEE European Solid-State Device Research Conference (ESSDERC), 2002, pp. 567-570.

[9] F.Irrera, B. Ricco, "Pulsed tunnel programming of nonvolatile memories", IEEE Trans. On Electron Devices, vol.50, No.12, December 2003, pp. 2474-2480.

[10] A.Chimenton, F.Irrera, P.Olivo, "Improving performance and reliability of NOR-Flash arrays by using pulsed operation", Microelectronics Reliability, vol.46, 2006, pp. 1478-1481.

[11] F.Irrera, T.Fristachi, D.Caputo, B.Ricco, "Optimising Flash memory tunnel programming", Microelectronics Engineering, vol.72, 2004, pp. 405-410.

[12] P.Canet, R.Bouchakour, J.Razafindramora, F.Lalande, J.M.Mirabel, "Very fast EEPROM erasing study", Proc. of IEEE European Solid-State Circuit Conference (ESSCIRC), 2002, pp. 683-686.

[13] Keysight Technologies, Keysight B1500A Data Sheet, February 2016.

[14] V.Della Marca, J.Postel-Pellerin, G.Just, P.Canet, J-L.Ogier, "Impact of endurance degradation on the programming efficiency and the energy consumption of NOR Flash memories", Microelectron. Reliab., vol.54, No.9-10, 2014, pp. 2262-2265.

[15] V.Della Marca, T.Wakrim, J.Postel-Pellerin, "Advanced experimental setup for reliability and current consumption measurements of Flash non-volatile memories", Proc. Of the 20th IMEKO TC4 International Symposium, 2014, pp. 1036-1040.

[16] B.Rebuffat, P.Masson, J-L.Ogier, M.Mantelli, R.Laffont, "Effect of AC stress on oxide TDDB and trapped charge in interface states" Proc. of International Symposium on Integrated Circuits (ISIC), 2014, pp. 416-419.

[17] American Department of Defense, Military handbook – Reliability prediction of electronic equipment (mil-hdbk-217F), 1991.

[18] U.Gurel, M.Cakmakci, "Impact of reliability on warranty: A study of application in a large size company of electronics industry", Measurement, vol. 46, 2014, pp. 1297-1310.

[19] M.Catelani, L.Ciani, S.Rossin, M.Venzi, "Failure rates sensitivity analysis using Monte Carlo simulation", Proc. Of the 13th IMEKO TC10 Workshop on Technical Diagnostics, 2014, pp. 195-200.

[20] L.Ciani, M. Catelani, "A fault tolerant architecture to avoid the effects of Single Event Upset (SEU) in avionics applications", Measurement, vol. 54, 2014, pp. 256-263.

[21] M.Venzi, S.Rossin, C.Michelassi, C.Accillaro, M.Catellani, L.Ciani, « Improved FBD and RBD generation for system reliability assessment", Proc. Of the 12th IMEKO TC10 Workshop on Technical Diagnostics, 2013, pp. 266-270.

[22] C.Calaiselvan, L.Rao, "Accelerated life testing of nano ceramic capacitors and capacitor test boards using non-parametric method", Measurement, vol. 88, 2016, pp. 58-65.