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Mixed baseband architecture based on FBD ΣΔ–based ADC for multistandard receivers

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ABSTRACT
This paper presents the design and simulation results of a novel mixed baseband stage for a frequency band decomposition (FBD) analog-to-digital converter (ADC) in a multistandard receiver. The proposed FBD-based ADC architecture is flexible with programmable parallel branches composed of discrete time (DT) 4th order single-bit ΣΔ modulators. The mixed baseband architecture uses a single non-programmable anti-aliasing filter (AAF) avoiding the use of an automatic gain control (AGC) circuit. System level analysis proved that the proposed FBD architecture satisfies design specifications of the software defined radio (SDR) receiver. In this paper, the authors focus on the Butterworth AAF filter design for a multistandard receiver. Besides, theoretical analysis of the reconstruction stage for UMTS test case is discussed. It leads to a complicated system of equations and high digital filter orders. To reduce the digital reconstruction stage complexity, the authors propose an optimized digital reconstruction stage architecture design. The demodulation-based digital reconstruction stage using two decimation stages has been implemented using MATLAB/SIMULINK. Technical choices and performances are discussed. The computed signal-to-noise ratio (SNR) of the MATLAB/SIMULINK FBD ADC model is equal to at least 75 dB which satisfies the dynamic range required for UMTS signals. Next to hardware implementation with quantized filters coefficients, the authors implemented their proposition in VHDL in a SysGen environment. The measured SNR of the hardware implementation is equal to 74.08 dB which satisfies the required dynamic range of UMTS signals.

Section: RESEARCH PAPER

Keywords: Frequency band decomposition (FBD); ΣΔ modulators; software defined radio (SDR) receiver

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1. INTRODUCTION

Software defined radio (SDR) is a state-of-the-art technology solution of the software radio concept, first introduced by Mitola [1]. SDR was proposed by scientists to achieve a feasible multistandard receiver. To ensure software reconfigurability, the received signals must be digitized as near as possible to the antenna in order to reduce analog circuitry. This leads to increased design constraints of the analog-to-digital converter (ADC). In fact, in literature, there is no fully integrated ADC that covers different coexisting wireless and mobile standards from narrowband to wideband channels with different required dynamic ranges [2]. To deal with this problem, the authors propose the use of parallel architectures of ΣΔ modulators that ensure high accuracy, in terms of dynamic range, while extending conversion bandwidth.

Parallel architectures have become an attractive solution for analog-to-digital conversion especially in the context of SDR, where new applications require extended bandwidths. There are three main parallel architectures described in the literature; the Hadamard modulated parallel architecture (ΠΣΔ) [3], the time-interleaved architecture (ΤΙΣΔ) [4], and the frequency band decomposition (FBD) architecture [5]-[7]. In this paper, the authors choose for the FBD architecture because unlike ΠΣΔ and ΤΙΣΔ architectures the FBD architecture is insensitive to gain and offset mismatches [8], [9]. In the FBD architecture, the parallel ΣΔ modulators are band-pass (BP) and each one converts a part of the total input signal band. There are propositions of FBD architecture designs in the literature, essentially in [5]-[7]. The main drawback of these solutions is

that they are based on continuous-time (CT)- ΣΔ modulators. In fact, CT-ΣΔ modulators bring analog errors that should be handled in the digital reconstruction stage. To overcome this problem, the authors proposed an FBD architecture based on discrete-time (DT)- ΣΔ modulators [10]. They are 4th order ΣΔ modulators based on single-bit quantizers [10]. The authors choose single-bit quantization to overcome non-linearity errors introduced by multi-bit quantizers [7]. Moreover, the novelty in this proposed architecture is the use of six programmable parallel branches with different sub-bandwidths, where only some branches are active according to the selected standard. The multistandard receiver handles E-GSM, UMTS and IEEE802.11a communication standard signals. The outputs of the parallel branches in the FBD ADC architecture have to be recombined using a digital reconstruction stage to provide the overall final output. E-GSM signals are not concerned in this stage since they solicit only one branch of the FBD ADC architecture. Only decimation is required at the ΣΔ modulator output. However, a digital reconstruction stage is mandatory for the UMTS and IEEE802.11a signals that solicit the three first branches and all the six branches of the ADC architecture, respectively.

In [11], the authors focused on the design and test of a digital reconstruction stage for the FBD ΣΔ-based ADC architecture. It was verified when implementing the whole ADC architecture in MATLAB/SIMULINK that the architecture performances satisfy the standard requirements for the dynamic range of the UMTS signals in this test case. The choice of this test case has been made because the three first branches of the ADC architecture, which are activated for digitizing UMTS signals, are reused for the digitization of IEEE802.11a signals. Besides, the UMTS standard requires a dynamic range of 73.8 dB that is higher than the required dynamic range for IEEE802.11a which equals 61.8 dB.

In this paper, interest is focused on the design of the mixed baseband stage for the SDR receiver. Indeed, in a conventional baseband receiver stage, an anti-aliasing filter (AAF), an Automatic Gain Control (AGC) circuit and an ADC are required to analogically process and digitize the received signals. However, in the proposed mixed baseband stage solution in this paper, the authors suggest to suppress the AGC, to design a single passive AAF and to digitize the received signal thanks to the multistandard FBD DT ΣΔ-based ADC architecture. Moreover, the theoretical analysis of the digital reconstruction stage based on demodulation is detailed using multirate theory. The design of the FBD ΣΔ-based ADC with demodulation-based digital reconstruction stage is first recalled [11]. Then, the novelty comes with the theoretical discussion that justifies the authors' proposition of an optimized digital reconstruction stage. In this paper, the authors come also with new comparative MATLAB/SIMULINK simulation results of signal-to-noise ratio regarding frequency position of the input signals. Besides, results of hardware implementation with quantized filter coefficients are presented and discussed.

The paper is organized as follows. In Section 2, the design of an FBD ΣΔ-based mixed baseband stage with a single passive AAF ahead intended for an SDR receiver is presented. Section 3 deals with the digital reconstruction stage of the FBD ΣΔ-based ADC. The two existing approaches in the literature, the direct reconstruction and the demodulation-based reconstruction, are discussed. A demodulation based digital reconstruction stage design for UMTS test case is proposed and analyzed theoretically using multirate theory. This initial design has been modified and optimized in order to allow its implementation. Simulation results of the FBD ΣΔ-based ADC model using the MATLAB/SIMULINK environment are presented in Section 4. Then, implementation results in VHDL using the SysGen environment are presented and discussed. Finally, some conclusions are drawn in Section 5.

2. FLEXIBLE FBD ΣΔ ARCHITECTURE DESIGN

To reach system level specifications of wireless and mobile standards, the authors propose to use a parallel ΣΔ modulator architecture and modify the conventional mixed baseband stage design [10].

The multistandard receiver processes E-GSM [13], UMTS [14] and IEEE802.11a [15] communication signals [10]. According to these supported communication standard specifications, design specifications for a multistandard SDR receiver have been computed. Furthermore, a hybrid homodyne/low-IF architecture was proposed in [16] for the SDR receiver front-end. An RF filter selects the received signals. Afterward, the signals are amplified by a low-noise amplifier (LNA). Then, on the one side, the UMTS and IEEE802.11a signals are down-converted by the mixer to baseband frequencies. On the other side, the E-GSM signals are down-converted to a low intermediate frequency of 100 kHz to overcome flicker noise disturbance. System level specifications are introduced in Sub-section 2.1. Then, in Sub-section 2.2, the mixed baseband stage design is explained. Next, the design of the non-programmable AAF is proposed in Sub-section 2.3. Afterwards, the design of the FBD ΣΔ-based ADC architecture is detailed in Sub-section 2.4.

2.1. Mixed baseband SDR receiver specifications

According to the specifications of the communication standards handled by the SDR receiver, system level specifications for the baseband receiver are depicted. Table 1 summarizes the channel bandwidth Ch_{BW}, the channel spacing Ch_{sp}, the reference sensitivity S_{ref}, the signal-to-noise ratio (SNR) at the receiver input, SNR_{in}, the signal-to-noise ratio at the receiver output SNR_{out}, the analog gain relative to a 13 dBm ADC full scale input G_{ana}, the receiver dynamic range DR_{in} and the ADC dynamic range DR_{ADC} from which the ADC resolution Res_{ADC}, is deduced.

Since E-GSM signals are down-converted to a low intermediate frequency of 100 kHz to avoid flicker noise, the E-GSM channel bandwidth is considered equal to 200 kHz.

The mixed baseband architecture is presented in the next sub-section.

Table 1. Design specifications for the E-GSM/UMTS/IEEE802.11a receiver.

	E-GSM	UMTS	IEEE802.11a
Ch_{BW} (MHz)	0.2	3.84	16.6
Ch_{sp} (MHz)	0.2	5	20
S_{ref} (dBm)	-102	-117	-65
SNR_{in} (dB)	18.8	-9	36.6
SNR_{out} (dB)	9	-18.2	26.6
G_{ana} (dB)	28	38	43
DR_{in} (dB)	87	92	35
DR_{ADC} (dB)	96	73.8	61.8
Res_{ADC} (bits)	16	12	10

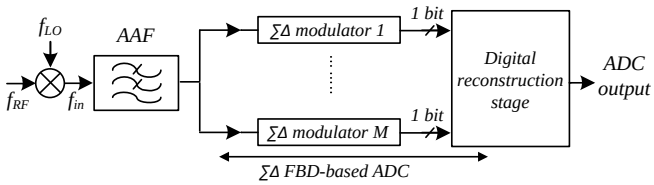

Figure 1. FBD ΣΔ-based mixed baseband stage.

2.2. Mixed baseband architecture

The mixed baseband stage, presented in Figure 1 [10], follows the mixer which is controlled by the local oscillator (LO). The mixed baseband stage is composed of a single passive low-pass (LP) AAF that precedes the FBD ΣΔ-based ADC. There is no need for n automatic gain control (AGC) circuit before the ADC stage since the AAF filters only E-GSM blockers that are outside the IEEE802.11a bandwidth [16]. The M parallel single-bit quantizer ΣΔ modulators are designed using Matlab tools. Their stability is ensured using a test plan performed in [10]. ΣΔ modulator outputs are combined in the digital reconstruction stage to reconstruct the final output.

The design of the non-programmable AAF is explained in the next sub-section.

2.3. Design of the non-programmable AAF

In this sub-section, the authors are interested in the design of a Butterworth non-programmable AAF for the SDR receiver. This AAF is unique for the E-GSM, UMTS and IEEE802.11a signals. Its role is to attenuate blockers and interfering signals which are susceptible to fold on the useful signal after sampling operation of the ADC, while ensuring the required SNR_{out} as defined by design specifications presented in Table 1.

The low-pass AAF is defined by its cut-off frequency f_p, its rejection frequency f_r, its maximal attenuation in the useful bandwidth A_{max}, and its minimal attenuation A_{min}, beyond the rejection frequency. The cut-off frequency is set equal to half of the channel bandwidth with a conception margin of 30 %. This margin is required to avoid attenuation in the useful channel bandwidth after analog integrated circuit realization but also circuit aging [16]. The rejection frequency is fixed at F_s-Ch$_{BW}$/2, where F_s is the sampling frequency. The F_s values for the different supported standards are obtained when designing the FBD ΣΔ-based ADC as given in Table 2 [10]. These evaluation conditions are explained by Figure 2.

The minimal attenuation is calculated as given by (1) [16],

$$A_{\min} = N_{bl} - S_{ref} + SNR_{out} + M_{AAF} \quad (1)$$

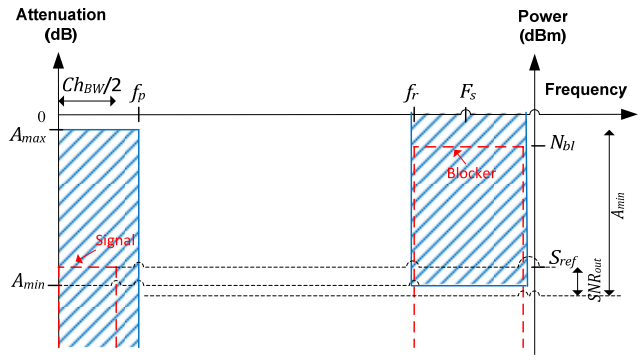

Figure 2. Evaluation conditions for the AAF design.

Table 2. Design of the LP AAF filter

	E-GSM	UMTS	IEEE802.11a
F_s (MHz)	72	72	96
f_p (MHz)	10.8	10.8	10.8
f_r (MHz)	71.8	70.08	85.2
N_{bl} (dB)	-23	-44	-47
A_{min} (dB)	85	51.8	41.6
AAF order (n)	6	4	3

where S_{ref} is the receiver sensitivity whose values for the different supported standards are given in Table 1, M_{AAF} is a margin of conception equal to 3 dB attributed to S_{ref}, and N_{bl} is the level of the blocker to attenuate. The blocker level is calculated given the blocker's profile at the RF filter output of the different supported standards. In fact, LNA and mixer linearly amplify the signals in the received bandwidth. Values of the AAF parameters are summarized in Table 2. The cut-off frequency is considered to be the same for the three standards and corresponds to half of the Ch_{BW} of IEEE802.11a standard with a margin of 30 %.

The AAF order is therefore computed given the Butterworth attenuation expression as described by (2),

$$A(f) = 10Log_{10}(1 + (10^{A_{\max}/10} - 1)(\frac{f}{f_p})^{2n}) \quad (2)$$

where n is the Butterworth filter's order to compute and A_{max} is set equal to 0.3 dB.

Given the needed A_{min} to attenuate blockers at the rejection frequency of each standard, the required AAF order is computed. Computation results are summarized in Table 2.

For UMTS and IEEE802.11a standards, the required AAF orders are 4 and 3, respectively. However, the E-GSM standard is the most restrictive since it requires a 6th order Butterworth AAF. Thus, for the SDR receiver the only AAF for the three standards is a 6th order Butterworth AAF. The frequency response of the designed AAF is presented in Figure 3.

2.4. Flexible FBD ΣΔ architecture

The authors in [10] started from SDR receiver specifications in terms of channel bandwidths and required ADC dynamic ranges for the chosen communication standards. The designed discrete-time (DT) FBD ΣΔ architecture for the ADC stage was proposed in [10]. The design realizes a trade-off between increasing the sampling frequency while still operating in discrete time and increasing the number M of parallel branches regarding a low-complexity goal, or increasing ΣΔ modulator orders while keeping them stable. Thus, an FBD ΣΔ architecture which is composed of 6 programmable parallel

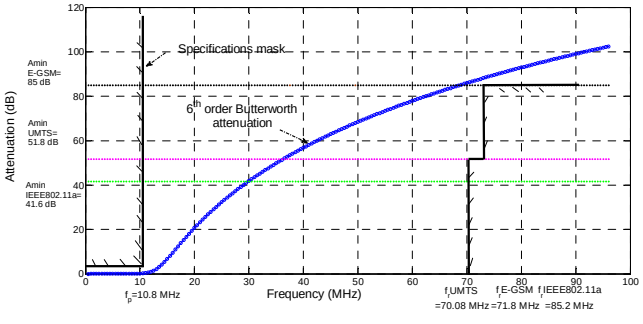

Figure 3. Frequency response and specification mask of the LP non-programmable AAF for the SDR receiver.

branches was proposed as presented in Figure 4(a).

According to the E-GSM, UMTS or IEEE802.11a communication standard, from the whole architecture only the needed branches are activated. Each branch is composed of a DT 4th order single-bit quantizer ΣΔ modulator. The ΣΔ modulator order is defined as the number of integrators or resonators k for low-pass (LP) and band-pass (BP) ΣΔ modulators, respectively. Since the designed FBD architecture is composed of both LP and BP ΣΔ modulators, the authors designate in this paper k as ΣΔ modulator order [10]. Besides, the ΣΔ modulators of the proposed FBD architecture are based on a non-unitary signal transfer function (NU-STF) that permits dealing with stability problems and recovering the input signal dynamic range [10]. The branch bandwidths are different and the sampling frequencies vary from one radio communication standard to another in order to optimize the flexible FBD ΣΔ architecture while fulfilling the theoretically required dynamic ranges. The branch bandwidth and the sampling frequency according to the chosen standard are given by the branch frequency division plan presented in Figure 4(b).

In the next section, to detail the theoretical analysis and design of the digital reconstruction stage of the FBD ΣΔ-based architecture, the authors select the UMTS standard as a test case. The choice of this test case has been made because the UMTS standard uses the three first branches of the ADC architecture. These branches are also selected with three more branches for the digitization of IEEE802.11a signals. Moreover, the required standard dynamic range of the UMTS is equal to 73.8 dB which is higher than the 61.8 dB for the required dynamic range of the IEEE802.11a.

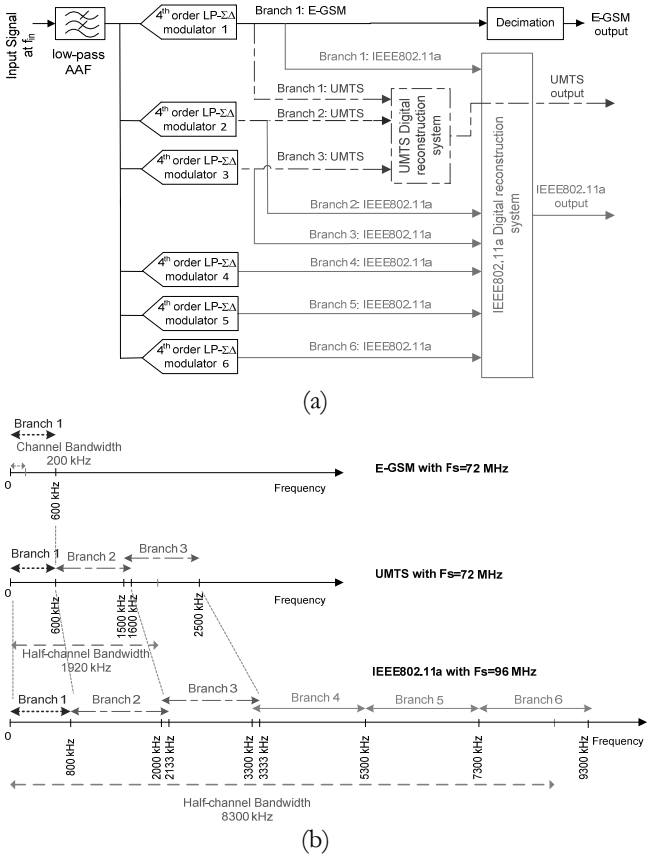

Figure 4. (a) Designed FBD ΣΔ–based ADC architecture, (b) branch frequency division plan.

3. DIGITAL RECONSTRUCTION STAGE: THEORETICAL ANALYSIS AND DESIGN

In the literature, there are two main approaches to reconstruct the output signal from the parallel ΣΔ modulator outputs while ensuring the required dynamic range [5]. For the first solution, the ΣΔ modulator outputs are directly processed using band-pass filters, then, the selected signals are decimated. However, the second solution demodulates each ΣΔ modulator output signal by converting it to baseband frequencies, then, the signal is decimated before being processed by a low-pass filter. It was shown in [5] that the digital reconstruction with direct processing presents high complexity due to high required BP filter orders and operating sampling frequencies. The digital reconstruction with demodulation requires lower LP filter orders and operating sampling frequencies. Consequently, in this paper, the authors proceed to digital reconstruction with demodulation whose architecture is explained in sub-section 3.1. The theoretical analysis of this architecture is presented in Sub-section 3.2. Afterwards, an optimized digital reconstruction stage is implemented using MATLAB/SIMULINK and technology choices are discussed in Sub-section 3.3.

3.1. Digital reconstruction with demodulation

The digital reconstruction architecture with demodulation is presented in Figure 5. In this digital processing, the BP ΣΔ modulator output signals are first brought to baseband by processing a complex demodulation. This operation consists in multiplying modulator outputs by the complex sequence $m_k[n]$ as given by (3) where f_{ck} is the central frequency of the kth branch bandwidth, T_s is the sampling period which is equal to $1/F_s$ and n is a positive integer:

$$m_k[n] = e^{-j2\pi f_{ck} n T_s} . \quad (3)$$

Since the ΣΔ modulators oversample input signals [5], it is mandatory to proceed to decimation and filtering operations after the complex demodulation operation. Hence, each demodulated signal is decimated in order to decrease its sampling frequency and bring it to the Nyquist frequency which is defined as the double of the channel bandwidth. The global decimation factor D is equal to the global oversampling ratio, OSR, defined as the sampling frequency F_s, out of the Nyquist frequency. Then, each demodulated and decimated signal is processed by a low-pass filter that selects the branch bandwidth before being modulated. The modulation operation consists in frequency up-converting each baseband signal around the corresponding branch central frequency at the Nyquist frequency. Finally, the output signals of the parallel branches are recombined to form the output signal of the FBD architecture. For the first branch that operates with a LP-ΣΔ

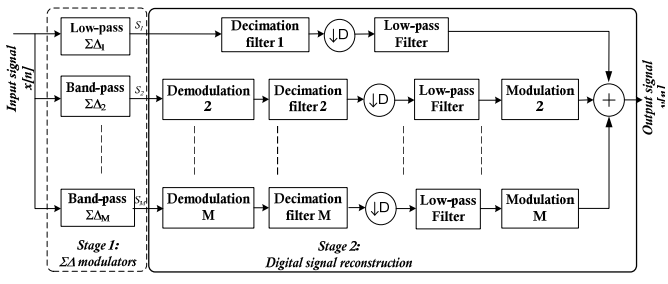

Figure 5. Digital reconstruction with demodulation of the FBD architecture (general case).

modulator, there is no need to demodulate and modulate as shown in Figure 5.

Starting from the test case corresponding to the FBD ΣΔ-based ADC architecture operating to digitize UMTS signals, the design of a demodulation based digital reconstruction stage is performed. In this chosen test case, only the three first parallel branches of the FBD ADC architecture are activated. The sampling frequency is set at 72 MHz and operating branche bandwidths are as explained by the branch frequency division plan for UMTS signals presented in Figure 4(b). The global decimation factor D is chosen equal to 16 which is an integer number that permits digitizing UMTS signals at a Nyquist frequency equal to 4.5 MHz. This Nyquist band is between the channel bandwidth Ch_{BW} and the channel spacing Ch_{sp}, as given in Table 1. The equivalent diagram in the discrete-time domain of the designed digital reconstruction stage is presented in Figure 6 where $H_k(z)$ is the non-unitary signal transfer function of the k^{th} ΣΔ modulator, $G_k(z)$ the decimation filter of the k^{th} branch, and $F_k(z)$ the branch bandwidth selection filter of the k^{th} branch.

This model is analyzed analytically in the next sub-section.

3.2. Theoretical study of the demodulation-based digital reconstruction stage

In this sub-section, based on the multirate theory [12], the theoretical analysis of the digital reconstruction stage model, designed for the UMTS test case as presented in Figure 6, is accomplished. In the first branch, a decimation operation and branch selection filtering process are performed. It is necessary to start by presenting the general expression of the z-transform of a decimated input signal by a decimation factor D as given by (4) [16]:

$$Y(e^{j\omega})=\frac{1}{D}\sum_{l=0}^{D-1}X(e^{j(\omega-2\pi l)/D}) \quad or \quad Y(z)=\frac{1}{D}\sum_{k=0}^{D-1}X(z^{1/D}W^l) \tag{4}$$

with $W=e^{-j2\pi/D}$ and $z=e^{j\omega}$. Therefore, the transfer function of the first branch output signal is deduced as expressed by equation (5):

$$Y_1(z)=\frac{1}{D}\sum_{l=0}^{D-1}X(z^{1/D}W^l)\times H_1(z^{1/D}W^l)G_1(z^{1/D}W^l)F_1(z^{1/D}) \tag{5}$$

In the 2nd and 3rd branche, the digital reconstruction processing contains demodulation and modulation operations that consist, as explained in the previous sub-section, in multiplication of the signal by a discrete exponential signal as given by (3). It is important to note that in this designed digital reconstruction stage, demodulation is operated at the ΣΔ modulator oversampling frequency F_s. However, the modulation is performed at the down sampling frequency equal to F_s./D. Therefore, the modulation is obtained by multiplying the outputs of branch selection bandwidth filters by the sequence given by (6):

$$m_{\mathrm{mod}\_k}[n]=e^{j2\pi f_{ck}nDT_s}. \tag{6}$$

The z-transform expression of the 2nd branch output signal after demodulation Y_{2dem}, is then given by expression (7):

$$Y_{2dem}(z)=X(z\ \ e^{j2\pi f_{c2}T_s})H_2(z\ \ e^{j2\pi f_{c2}T_s}). \tag{7}$$

Then, the expression of the 2nd branch output after decimation is expressed by (8):

$$Y_{2dec}(z)=\frac{1}{D}\sum_{l=0}^{D-1}X(z^{1/D}.W^l.e^{j2\pi f_{c2}T_s/D})\times \times H_2(z^{1/D}.W^l.e^{j2\pi f_{c2}T_s/D})G_2(z^{1/D}.W^l) \tag{8}$$

Therefore, the z-transform expressions of the 2nd and 3rd branch output signals are determined as given respectively by (9) and (10):

$$\begin{aligned}Y_2(z)=\frac{1}{D}\sum_{l=0}^{D-1}&X(z^{1/D}.W^l.e^{-j2\pi f_{c2}T_s(D-1)/D})\times\\&\times H_2(z^{1/D}.W^l.e^{-j2\pi f_{c2}T_s(D-1)/D})\times\\&\times G_2(z^{1/D}W^l e^{-j2\pi f_{c2}T_s})F_2(z^{1/D}e^{-j2\pi f_{c2}T_s})\end{aligned} \tag{9}$$

$$\begin{aligned}Y_3(z)=\frac{1}{D}\sum_{l=0}^{D-!}&X(z^{1/D}.W^l.e^{-j2\pi f_{c3}T_s(D-1)/D})\times\\&\times H_3(z^{1/D}.W^l.e^{-j2\pi f_{c3}T_s(D-1)/D})\times\\&\times G_3(z^{1/D}.W^l.e^{-j2\pi f_{c3}T_s})F_3(z^{1/D}e^{-j2\pi f_{c3}T_s})\end{aligned} \tag{10}$$

The combined output signal of the FBD ADC architecture is obtained by summing the three branche output signals as presented by (11):

$$Y(z)=Y_1(z)+Y_2(z)+Y_3(z). \tag{11}$$

To cancel the aliasing and ensure a perfect reconstruction system, the output signal has to be a delayed version of the input signal and the alias terms should be canceled [12]. In the filter bank architectures, the signal is decimated at the input of the converters and interpolated at their outputs. The main difference between the FBD architecture with demodulation-based digital reconstruction and the filter bank architecture is the presence of demodulation and modulation operations. In fact, the signal at each band-pass branch is frequency shifted through these operations around the corresponding branch's central frequency. Consequently, a part of the input signal which is frequency shifted around the branch central frequency is applied at each branch's bandwidth. There is a need to recuperate these input signals at the recombined final output. However, the aliasing terms introduced by decimation and corresponding to the input signal terms for l different from zero have to be eliminated to ensure perfect reconstruction. This leads to the expression of the output signal as given by (12) and (13):

$$Y(z)=\frac{1}{D}\sum_{l=0}^{D-1}\sum_{k=1}^{M}\begin{bmatrix}X\left(z^{1/D}W^lV_k^{(D-1)/D}\right)\times\\H_k\left(z^{1/D}W^lV_k^{(D-1)/D}\right)\times\\G_k\left(z^{1/D}W^lV_k^{(D-1)/D}\right)\times\\F_k\left(z^{1/D}V_k\right)\end{bmatrix} \tag{12}$$

where $V_k=e^{-j2\pi f_{ck}T_s}$ with $f_{c1}=0$

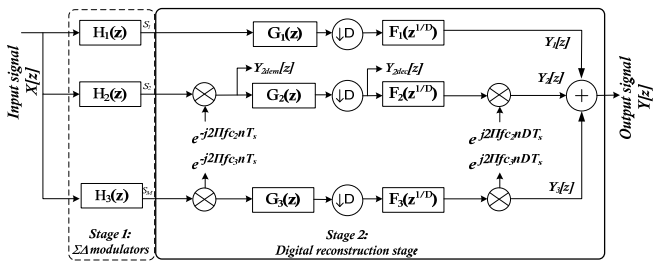

Figure 6. Equivalent diagram of demodulation-based digital reconstruction stage model for the UMTS use case.

$$For \quad l=0,$$

$$Y(z)=\frac{1}{D}\sum_{k=1}^{M}\begin{bmatrix} X\left(z^{1/D}V_k^{(D-1)/D}\right) & H_k\left(z^{1/D}V_k^{(D-1)/D}\right)\times \\ G_k\left(z^{1/D}V_k^{(D-1)/D}\right) & F_k\left(z^{1/D}V_k\right) \end{bmatrix} \tag{13}$$

$$=\frac{1}{D}\sum_{k=1}^{M}\alpha_k z^{-\delta_k} X\left(z^{1/D}V_k^{(D-1)/D}\right)$$

$$For \quad l\neq 0, \qquad Y(z)=0$$

where α and δ are gain and delay, respectively.

This theoretical design of the digital reconstruction stage leads to a complex system of equations and also to very high filter orders when implementing it on MATLAB/SIMULINK. Consequently, it is essential to modify this model to permit an optimized digital implementation solution.

3.3. Proposed optimized digital reconstruction stage architecture design

The digital reconstruction architecture based on demodulation for the UMTS test case presented in Sub-section 3.1 has been modified in order to minimize its implementation complexity. The optimized design is detailed in this sub-section. The model of the FBD ΣΔ-based ADC with the proposed digital reconstruction architecture is designed using MATLAB/SIMULINK as presented in Figure 7. The model corresponds to the test case of the FBD architecture intended for UMTS signals. The corresponding bloc diagram for this model is presented in Figure 8.

For the first branch, only decimation and filtering operations are needed for the digital reconstruction since it operates at low-pass frequencies as shown in Figure 5.

The decimation operation is always preceded by a decimation filter that serves as an anti-aliasing filter of the re-sampling operation. To reduce the complexity of such a decimation filter with a high decimation factor, the authors opt for two-stage decimation. The first stage ensures decimation by a factor of 8 when the second stage decimates by a factor of 2.

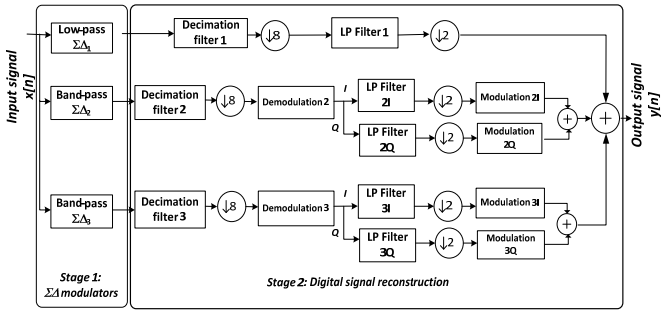

Figure 8. Block diagram of FBD ΣΔ-based ADC architecture with demodulation-based digital reconstruction .

For the second and third parallel branches that operate in band-pass frequencies, the digital reconstruction is composed of the operations of demodulation, decimation, filtering and modulation as explained in Figure 5. The complex demodulation as explained before consists in multiplying the ΣΔ modulator output by a discrete exponential signal at the branch central frequency as given by (1). In the MATLAB/SIMULINK model, the authors replace the complex demodulation and modulation by in phase (I) and quadrature (Q) paths to ensure better conditions for implementation.

The demodulation should then be followed by filtering of the unwanted frequencies which are due to the demodulation operation. This filter presents high complexity since the unwanted frequencies are at low values and the filter operates at the oversampling frequency of the ΣΔ modulator. For the second branch, the required finite impulse response (FIR) filter order after demodulation is equal to 190. To deal with this problem, the authors opt to place the demodulation operation after the first decimation stage with a factor of 8. This solution

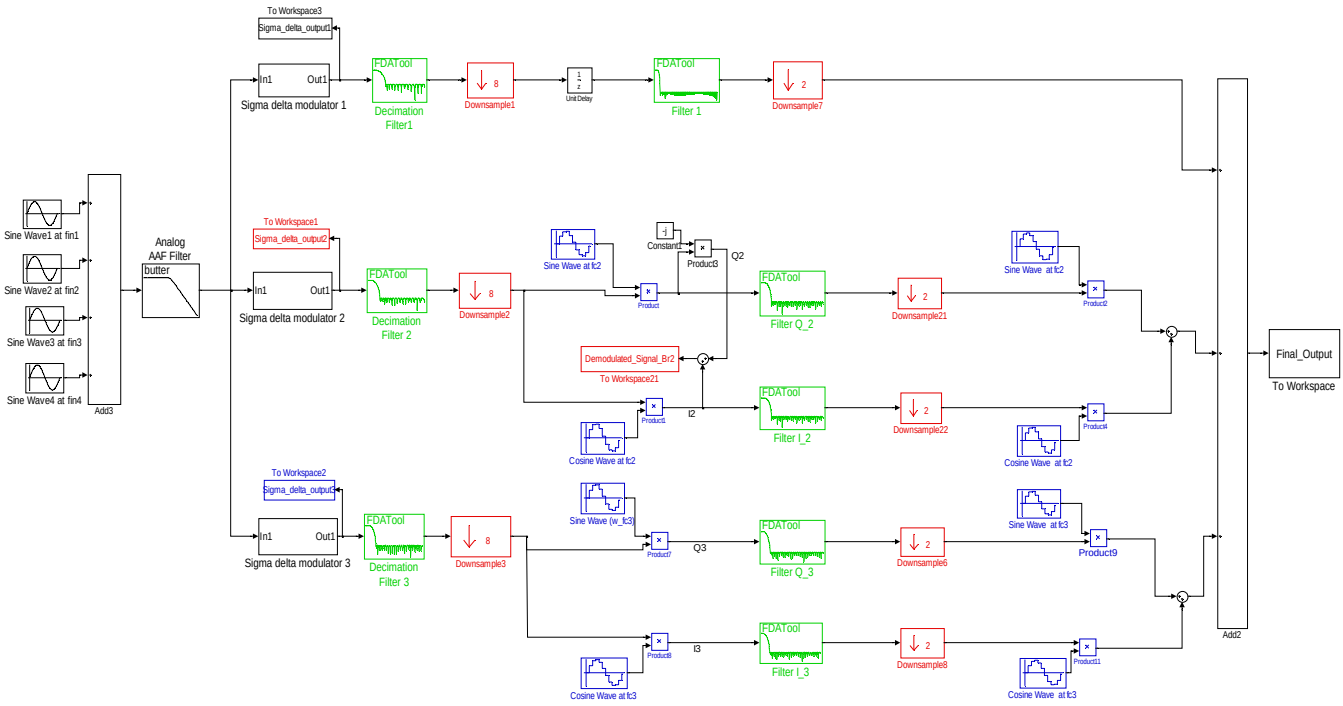

Figure 7. Proposed FBD-based ADC architecture model with demodulation-based digital reconstruction.

permits to reduce the operating frequency of the filter following the demodulation. Moreover, it allows combining this filter with the second stage decimation filter and the low-pass filter that selects the branch bandwidth signals and rejects the quantization noise at the adjacent branches bandwidths.

The first decimation stage placed at the ΣΔ modulator output is composed of an operation of decimation by a factor of 8 preceded by a LP FIR decimation filter.

The order of these filters at the first, second and third branches are chosen to be 29, 39 and 56, respectively. Then, the order of the LP FIR filters of branch bandwidth selection are equal to 82.

The frequency response of these filters after modulation of the second and third ones is presented in Figure 9. The filter responses are overlapping. Their intersection is at a level around −6 dB and at the frequency limits between adjacent branches as shown in Figure 9.

The sum of the LP filters of 82nd order after modulation is computed and its frequency response magnitude is presented in Figure 10(a). At the higher and lower ends of the bandwidth, the magnitude response presents ripples and attenuations that do not exceed 2 dB as shown in Figure 10 (b). Thus, expected performances of the reconstruction system are not affected.

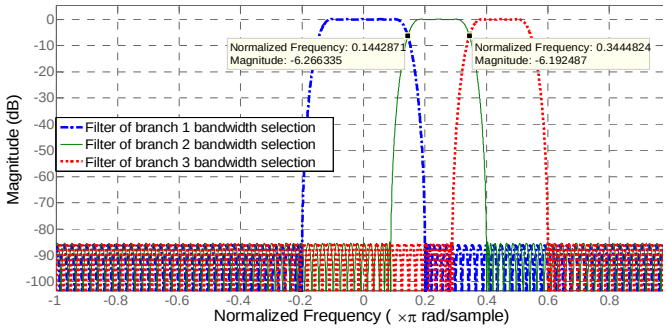

Figure 9. Magnitude of the LP filters of 82nd order after modulation.

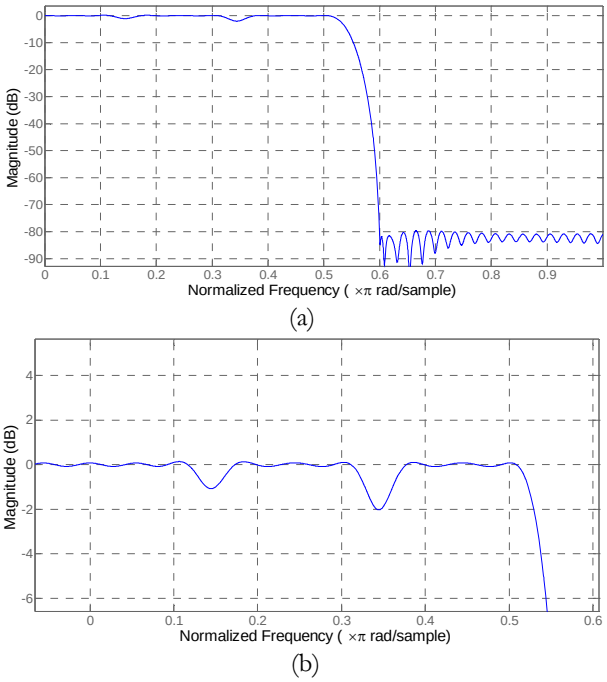

Figure 10. (a) Magnitude of the sum of LP filters of 82nd order after modulation, (b) zoom in [0, 0.6] normalized frequency band to show ripples.

After decimation and filtering operations, the I and Q paths are modulated to convert the sub-band signal frequency around its original frequency which is the branch central frequency. Finally, the sub-band output signals are recombined to obtain the reconstructed UMTS signal. Simulation results are presented in Section 4.

4. SIMULATION RESULTS

Simulation results are realized by applying a multi-tone signal composed of four sine-wave signals to the FBD model shown in Figure 7. The first and last sine-wave frequencies are placed in the bandwidths [0, 600 kHz] and [1500 kHz, 2500 kHz] of the branches 1 and 3, respectively. The selected values are 300 kHz and 1900 kHz. The first branch central frequency f_{c1} and the third branch central frequency f_{c3} are equal to 300 kHz and 2000 kHz, respectively. The two other sine waves are at frequencies in the 2nd branch bandwidth. They are situated on both sides of the 2nd branch central frequency f_{c2}, which is equal to 1100 kHz, and their values are 700 kHz and 1300 kHz.

In fact, the authors tested the UMTS FBD second branch with a two-tone signal to verify the correct operation of the I/Q demodulation and modulation stages. The sine-wave normalized amplitudes are set at 0.5 for the first and last sine waves and at 0.25 for the sine-waves of the 2nd branch where the normalized amplitude is the input amplitude out of the power supply voltage [10].

The zoom in the spectrum over [−4.5, 4.5 MHz] of the second branch sigma delta modulator output, Sigma_delta_output2, is drawn in Figure 11. It is shown that the sine-wave signals are at the frequencies 700 kHz and 1300 kHz as in the test conditions. To present I/Q demodulated signal of the 2nd branch as in Figure 11, the authors need to recombine a complex demodulated signal, Demodulated_Signal_Br2, as defined in Figure 7.

The sampling frequency after the first decimation stage is equal to 9 MHz and the spectrum covers the band [−4.5 MHz, 4.5 MHz]. The obtained sine-wave signals have frequencies 200 kHz and −400 kHz which are the frequencies of the needed demodulated sine-wave signals. However, the sine-wave signals at the frequencies −1800 kHz and −2400 kHz are unwanted signals that are filtered thanks to the filters FilterI_2 and FilterQ_2 following the demodulation stage.

After the second decimation stage, the recombined final output signal spectrum in the band [−2.25 MHz, 2.25 MHz] is presented in Figure 12. It shows that the modulated signals

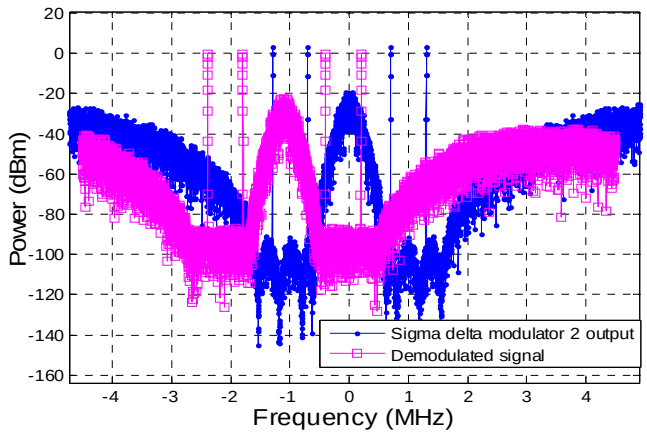

Figure 11. Demodulated signal spectrum of the 2nd branch.

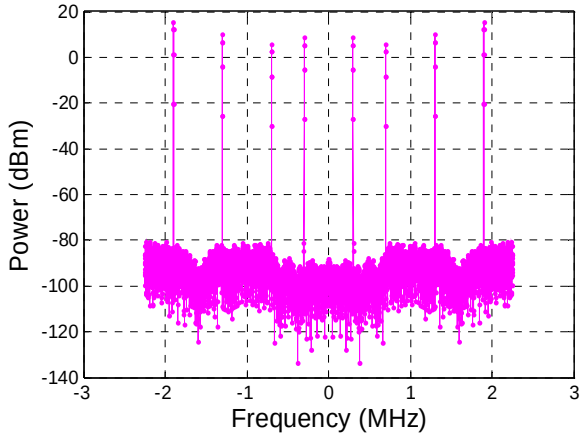

Figure 12. Recombined output signal spectrum.

have frequencies equal to ±300 kHz, ±700 kHz, ±1300 kHz and ±1900 kHz which corresponds to the chosen values of the test conditions of the simulation results. Moreover, the signal-to-noise ratio (SNR) computed using MATLAB/SIMULINK is equal to 75.06 dB which satisfies the required UMTS dynamic range which is equal to 73.8 dB.

Performance parameters as *SNR* and effective resolution Res_{ADC} are computed for different combination of input frequencies of the four sine-wave signals. Computation results are summarized in Table 3. Besides, the designed FBD model is implemented in VHDL using the System Generator (SysGen) tool from Xilinx Inc. in a co-simulation environment with MATLAB. The implementation is realized on a Virtex-6 FPGA target from Xilinx Inc. Test conditions for input signals are the same as for the MATLAB/SIMULINK simulation. The output signal spectrum is presented in Figure 13. The computed SNR for this spectrum is equal to 74.08 dB which satisfies the UMTS required dynamic range.

5. CONCLUSIONS

In this paper, the authors proposed a mixed baseband architecture based on a FBD ΣΔ–based ADC in a multistandard receiver. The mixed baseband stage architecture is presented and the single non-programmable AAF is designed using Butterworth approximation.

The theoretical analysis and design of the digital reconstruction stage for the FBD ΣΔ-based ADC architecture dedicated to multistandard radio receivers are proposed. The designed digital reconstruction stage is based on demodulation that brings the ΣΔ modulators outputs to baseband before proceeding to the decimation and LP filtering operations. The parallel signals are then modulated and combined to form a final output signal. However, the theoretical analysis of the digital reconstruction stage does not converge to a solution of filter coefficients. Besides, the first proposed design leads to very high filter orders when implemented in MATLAB/SIMULINK. Consequently, it is essential to modify this model to permit an optimized digital implementation solution. Finally, the whole FBD ΣΔ-based ADC architecture model with the optimized digital reconstruction stage is implemented and tested for the UMTS test case in MATLAB/SIMULINK. Moreover, hardware implementation and test results in the SysGen environment are presented for quantized coefficient values. All obtained results satisfy at least the required UMTS dynamic range which is equal to 73.8 dB.

Table 3. Performance parameters of final output signal.

Input signals frequencies (kHz)	*SNR* (dB)	Res_{ADC} (bits)
300, 700, 1300 and 1900	75.06	12.18
400, 800, 1400 and 2000	74.73	12.12
500, 900, 1400 and 1900	74.43	12.07
100, 1000, 1400 and 1700	75.26	12.21

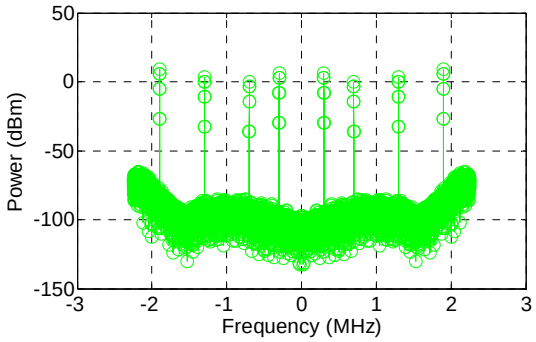

Figure 13. Frequency spectrum of the recombined output signal using SysGen implementation.

REFERENCES

[1] J. Mitola, "Software radios: survey, critical evaluation and future directions," IEEE Aero. and Elect. Syst. Mag., vol.8, no.4, pp.25-36, Apr. 1993.

[2] J. M. De la Rosa, "An empirical and statistical comparison of state-of-the-art sigma-delta-modulators," IEEE Int. Symp. on Circ. And Syst., ISBN 978-1-4673-5760-9, pp. 825-822, May 2013.

[3] I. Galton, H.T. Jensen, "Delta-sigma modulator based A/D conversion without oversampling," IEEE Trans. Circuits and Syst.-II: Analog and digital Sig. Proc., vol.42, no.12, pp.773-784, Dec. 1995.

[4] A. Eshraghi, T. Fiez, "A time-interleaved parallel ΔΣ A/D converter," IEEE Trans. Circuits and Syst.-II: Analog and digital Sig. Proc., vol.50, no. 3, pp.118-129, Mar. 2003.

[5] A. Beydoun, P. Benabes, "Bandpass/wideband ADC architecture using parallel delta sigma modulators", Proceedings of the 14th European Signal Processing Conf., Sept. 2006.

[6] P. Benabes, A. Beydoun, M. Javidan, "Frequency-band-decomposition converters using continuous-time Sigma Delta A/D modulators," IEEE North-East Workshop on Circuits and Syst. and TAISA Conf., pp. 1 – 4, Jun. 2009.

[7] P. Benabes, "Extended frequency-band-decomposition sigma-delta A/D converter", Analog Integr. Circ. Process., Springer Science+Business Media, LLC 2009.

[8] A. Eshraghi, T. Fiez, "A comparative analysis of parallel delta–sigma ADC architectures," IEEE Trans. Circuits and Syst. I: Regular Papers, vol. 51, no. 3, pp. 450 – 458, Mar. 2004.

[9] A. Blad et al., "A General Formulation of Analog-to-Digital Converters Using Parallel Sigma-Delta Modulators and modulation sequences", IEEE Asia Pacific Conf. Circuits and Syst. APCCAS, pp. 438-441, Dec. 2006.

[10] R. Lahouli, M. Ben-Romdhane, C. Rebai, D. Dallet, "Towards flexible parallel sigma delta modulator for software defined radio receiver", IEEE Int. Instrum. and Meas. Technology Conf., May 2014.

[11] R. Lahouli et al., "Digital reconstruction stage of the FBD ΣΔ-based ADC architecture for multistandard receiver", 20th IMEKO TC4 International Workshop on ADC Modelling and Testing Research on Electric and Electronic Measurement for the Economic Upturn, Benevento, Italy, Sept. 2014.

[12] P. P. Vaidyanathan, "Multirate Systems and Filter Banks," Eaglewood Cliffs, NJ: Prentice-Hall, 1993.

[13] GSM. Radio Transmission and Reception GSM 05.05. ETSI, 1996.

[14] UMTS. UE. Radio Transmission and Reception (FDD), 3GPP TS 25.101, Version 5.2.0 Release 5.ETSI 2002.

[15] IEEE 802.11a Part 11: Wireless LAN Medium Access Control (MAC), and Physical Layer Specifications, Amendment1 High Speed Physical Layer in the 5 GHz Band. IEEE, 1999.

[16] M. Ben-Romdhane, C. Rebai, A. Ghazel, P. Desgreys, P. Loumeau, "Nonuniformly Controlled Analog-to-digital Converter for SDR Multistandard Radio Receiver," IEEE Trans. Circuits and Syst. II: Brief Papers, vol. 58, no.12, pp. 862 – 866, Dec. 2011.