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Design and Implementation of 12-bit SAR ADC with Nanometer Technology

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Abstract

This work presents the design, synthesis, and physical implementation of a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) optimized for nanometer-scale CMOS technology. The architecture integrates a compact digital control unit, comparator interface, and DAC logic, synthesized using standard cell libraries under stringent timing and power constraints. Functional verification through waveform simulation confirms accurate bit cycling and convergence behavior across conversion phases. Post-synthesis analysis reports a silicon area of 409.374 μm² and a total dynamic power of 9321.018 nW, with leakage contributions minimized via multi-Vt cell deployment. Physical design using Cadence Innovus achieves a placed-and-routed layout with 1236.77 μm² footprint, adhering to foundry-specific DRC and LVS protocols. The final power profile, dominated by sequential logic, indicates a total consumption of 0.01931 mW, validating the design's suitability for low-power, high-resolution applications in advanced VLSI systems. This study demonstrates a scalable methodology for energy-efficient ADC integration in edge and mixed-signal platforms.

Keywords: 12-bit SAR, 45nm Technology, Functional Verification, Synthesis and Physical synthesis, Optimization

1. Introduction

Analog-to-Digital Converters (ADCs) serve as critical interfaces between analog environments and digital processing systems, enabling signal digitization in applications ranging from biomedical instrumentation to wireless communication and industrial automation [1]–[3]. Among various ADC architectures, the Successive Approximation Register (SAR) topology has gained prominence due to its inherent energy efficiency, moderate speed, and compact digital footprint [4], [5]. The SAR ADC operates by iteratively refining the digital output through binary search logic, making it particularly suitable for low-power, medium-resolution applications. As technology nodes scale below 65 nm, design challenges intensify due to increased leakage currents, reduced supply voltages, and variability in device characteristics [6], [7]. Recent advancements in nanometer CMOS processes have enabled tighter integration of mixed-signal components, allowing SAR ADCs to be synthesized entirely using digital standard cells [8], [9]. This digital-centric approach facilitates portability across technology nodes and simplifies physical design workflows. However, achieving high-resolution performance within constrained area and power budgets demands meticulous architectural optimization, including dynamic comparator design, low-capacitance DAC structures, and

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robust digital control logic [10]. Furthermore, timing closure and power integrity become critical during physical implementation, especially when targeting edge-deployable systems where thermal and energy constraints are stringent [11]. This study presents the complete design flow of a 12-bit SAR ADC implemented in a nanometer-scale CMOS process, encompassing behavioral modeling, RTL synthesis, power and timing analysis, and physical layout. The proposed architecture leverages standard cell-based synthesis and Innovus-driven place-and-route to achieve a compact footprint and low dynamic power consumption. Functional verification confirms accurate bit resolution and conversion timing, while post-layout analysis validates compliance with design rules and electrical integrity. The methodology outlined herein contributes to scalable, energy-efficient ADC design practices suitable for integration in next-generation VLSI platforms [12].

2. Literatue Survey

The SAR ADC architecture has undergone extensive evolution to meet the demands of low-power, high-resolution applications. Early implementations focused on binary-weighted capacitor arrays and asynchronous control logic to minimize energy consumption [1]. Innovations such as monotonic capacitor switching [2] and charge redistribution techniques [3] have significantly reduced switching energy, making SAR ADCs viable for battery-operated and implantable systems. These architectural refinements have enabled resolutions up to 12 bits while maintaining compact layouts and moderate sampling rates, particularly in sub-100 nm CMOS processes.

Recent research has emphasized digital calibration and redundancy techniques to enhance linearity and robustness against process variations. Xu et al. [4] introduced background calibration to correct capacitor mismatch dynamically, improving SFDR without increasing area overhead. Similarly, hybrid DAC structures combining capacitive and resistive elements have been proposed to balance speed and accuracy [5]. Comparator design has also seen substantial progress, with dynamic and zero-crossing comparators offering reduced offset and improved decision speed [6]. These developments collectively contribute to the feasibility of synthesizing SAR ADCs using digital standard cells, streamlining integration into digital SoCs.

Physical design considerations have gained prominence as SAR ADCs are increasingly deployed in edge and IoT platforms. Layout optimization techniques such as metal-aware placement, power rail partitioning, and via minimization are critical for maintaining signal integrity and thermal stability [7]. Moreover, leakage mitigation strategies like multi-threshold voltage (multi-Vt) cell usage and clock gating have proven effective in reducing standby power [8]. These studies underscore the importance of holistic design methodologies that span architecture, synthesis, and layout, especially when targeting nanometer-scale implementations with stringent power and area constraints.

3. Results and Discussions

1. Functional verification

Functional verification of the 12-bit SAR ADC was conducted using waveform simulation in Cadence, focusing on key signals such as and. The simulation timeline, measured in

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picoseconds, captures the dynamic behavior of the ADC during conversion cycles. Observing transitions in and corresponding updates in confirms the correct operation of the successive approximation algorithm. The signal flags the completion of each conversion, while ensures proper initialization. This visual inspection validates that the digital control logic, DAC interface, and comparator coordination function as intended, confirming the design's correctness before physical implementation.

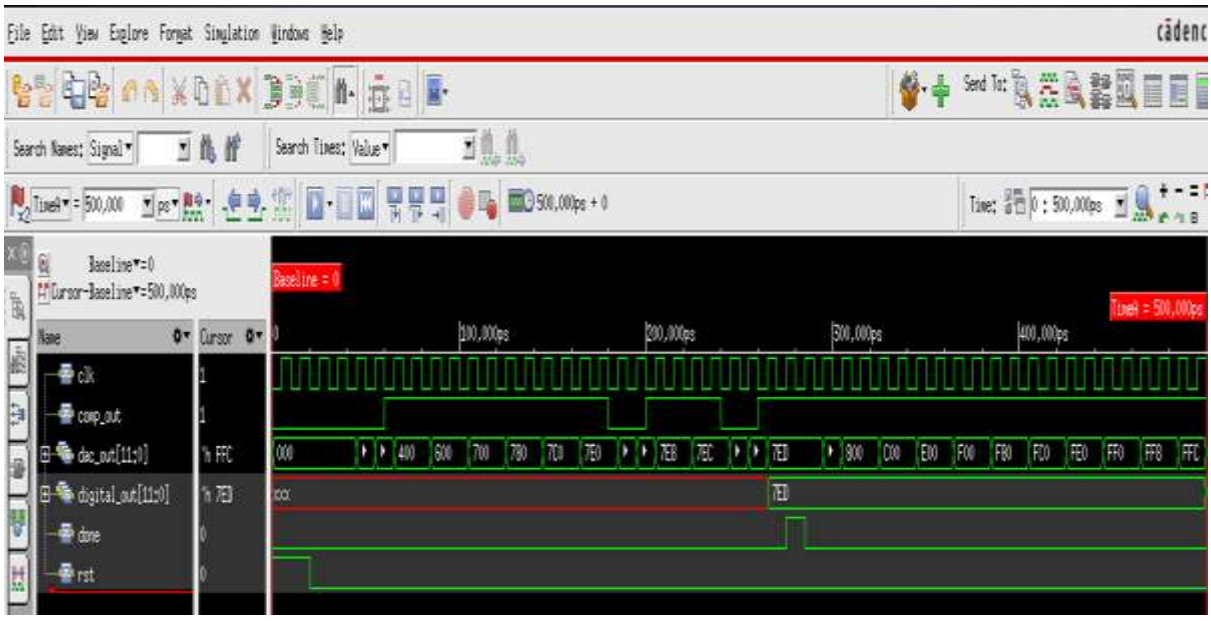

Figure 1: Functional verification of 12-bit SAR

Report Mapped Gates

Generated by: Genus(TM) Synthesis Solution 16.21-s018_1 (Feb 10 2017)
Generated on: Jun 16 2025 06:53:22
Module: design:sar_adc
Technology library: fast_vdd1v0 1.0
Operating conditions: PVT_1P1V_0C (balanced_tree)
Wireload mode: enclosed

Gate	Instances	Area	Library
OAI22XL	1	2.052	fast_vdd1v0
SDFFRHQX1	12	98.496	fast_vdd1v0
INVXL	10	6.840	fast_vdd1v0
NAND2BXL	4	5.472	fast_vdd1v0
OAI2BB1X1	10	17.100	fast_vdd1v0
NAND3X1	1	1.710	fast_vdd1v0
TOTAL	115	409.374	

Figure 2: Area Report

In the context of the 12-bit SAR ADC synthesized using nanometer technology, the area represents the total silicon real estate consumed by the digital logic components on the chip.

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According to the synthesis report, the design comprises 115 gate instances, collectively occupying 409.374 square micrometers. This includes various standard cells such as flip-flops (SDFFRHQX1), inverters (INVXL), and logic gates like NAND and OAI types, each contributing differently to the overall footprint. Efficient area utilization is crucial for compact layout, reduced parasitics, and lower fabrication costs, especially in advanced nodes where space is at a premium.

Power Details Report

Generated by: Genus(TM) Synthesis Solution 16.21-s018_1 (Feb 10 2017)
Generated on: Jun 16 2025 06:53:01
Module: design:sar_adc
Technology library: fast_vdd1v0 1.0
Operating conditions: PVT_1P1V_0C (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (n
sar_adc	115	22.859	7904.940	1416.078	9321.018

Figure 3: Power Report

The power analysis of the 12-bit SAR ADC synthesized in nanometer technology reveals a total switching power of approximately 9321.018 nW, indicating the dynamic energy consumed during signal transitions. Internal power, which accounts for energy dissipated within the cells due to charging and discharging of internal capacitances, stands at 7904.940 nW. Net power, representing the energy used by interconnects and routing, contributes 1416.078 nW. Additionally, leakage power—caused by subthreshold conduction and gate oxide tunneling in idle transistors is measured at 22.859 nW. These metrics, derived under the PVT_1P1V_0C condition using the fast_vdd1v0 library, are essential for evaluating the energy efficiency and thermal behavior of the ADC in real-world applications.

```
  Generated by:           Genus(TM) Synthesis Solution 16.21-s018_1
  Generated on:           Jun 16 2025  06:45:03 am
  Module:                 sar_adc
  Technology library:     fast_vdd1v0 1.0
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
```

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
bit_pos_reg[1]/CK				0		0	R
bit_pos_reg[1]/Q	DFFSHQX1	5	1.4	12	+57	57	F
g1772/A					+0	57	
g1772/Y	NOR2XL	3	0.9	26	+23	80	R
g1762/B					+0	80	
g1762/Y	NAND2XL	2	0.5	18	+21	100	F
g1759/A					+0	100	
g1759/Y	INVXL	2	0.6	11	+13	114	R
g1752/B					+0	114	
g1752/Y	NAND2XL	2	0.5	17	+15	129	F
g1746/B					+0	129	
g1746/Y	OR2X1	2	0.4	7	+28	157	F
g1727/B					+0	157	
g1727/Y	NOR2XL	12	7.2	159	+94	251	R
digital_out_reg[11]/SE	SDFFQX1				+0	251	
digital_out_reg[11]/CK	setup			0	+67	318	R

Figure 4: Timing Report

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The timing analysis of the 12-bit SAR ADC, synthesized using Genus™ Synthesis Solution, provides a detailed breakdown of signal propagation from the clock input of to the setup endpoint at . The report, generated under PVT_1P1V_OC conditions with the fast_vdd1v0 library, shows a sequence of logic elements including NOR, NAND, and inverter gates, each contributing incremental delays. Arrival times accumulate from 57 ps at the clock input to 318 ps at the output setup pin, with intermediate stages showing fanout, load, slew, and delay values. The timing slack is marked as "UNCONSTRAINED," indicating that no explicit constraints were violated, but also suggesting that formal timing closure may still be pending. This analysis is vital for verifying that the ADC operates reliably within its intended clock cycle, ensuring accurate bit resolution and conversion speed.

2. Synthesis

The synthesis of a 12-bit SAR ADC using nanometer technology involves translating the high-level design into a gate-level netlist optimized for area, speed, and power. Leveraging advanced synthesis tools, the digital control logic including the SAR register, comparator interface, and DAC control is mapped onto standard cells compatible with the target technology node. Timing constraints are carefully defined to ensure accurate bit cycling and decision-making within the conversion window. Power optimization techniques, such as clock gating and multi-Vt cell usage, are employed to minimize dynamic and leakage power. The result is a compact, high-resolution ADC core that meets stringent performance metrics, ready for placement and routing in a nanometer-scale VLSI environment.

Figure 5: Final Synthesis

3. Physical design

The physical design of the 12-bit SAR ADC using Cadence Innovus involves converting the synthesized netlist into a complete placed and routed layout, ensuring optimal performance and manufacturability. The layout includes standard cells for registers such as dac reg[5], adc reg[9], and state reg, which are strategically placed to minimize wirelength and timing delays. Power rails like vdd are distributed across multiple metal layers to ensure consistent power delivery throughout the chip. Routing is performed using several metal layers, with vertical

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and horizontal tracks optimized for signal integrity and minimal crosstalk. Vias are inserted to connect different metal layers, maintaining continuity and electrical reliability. The design strictly follows foundry-specific design rules, and comprehensive checks such as Design Rule Check (DRC) and Layout Versus Schematic (LVS) are executed to confirm physical correctness. This stage ensures that the digital logic synthesized earlier is accurately represented in silicon, making the design ready for tape-out and fabrication.

Figure 6: Final 12 Bit SAR Physical layout

he area report generated by the report area command in Innovus provides a summary of the physical footprint of the SAR ADC module. According to the output, the sar adc block contains 115 standard cell instances and occupies a total area of approximately 1236.77 square micrometers. This metric is crucial for evaluating layout density, optimizing die size, and estimating fabrication cost.

```
innovus 3> report_area
Depth   Name            #Inst   Area (um^2)
-------------------------------------------
0       sar_adc         115     1236.7746
1
```

Figure 7: Physical synthesis area report

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.01002	0.0003879	0.005475	0.01588	82.27
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.0005503	0.001752	0.001122	0.003424	17.73
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.01057	0.00214	0.006597	0.01931	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Default	0.9	0.01057	0.00214	0.006597	0.01931	100

Figure 8: Physical synthesis Power report

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The physical design power report for the SAR ADC reveals a total power consumption of approximately 0.01931 mW, broken down into internal, switching, and leakage components. Internal power dominates at 0.01057 mW (54.75%), followed by leakage power at 0.00660 mW (34.17%), and switching power at 0.00214 mW (11.08%). Sequential logic contributes the most, accounting for over 82% of the total power, while combinational logic adds around 17.73%. No power is consumed by macros, IOs, or clock networks in this report. These insights are essential for evaluating energy efficiency and guiding further optimization in low-power design strategies.

4. Conclusion

The design and implementation of a 12-bit SAR ADC in nanometer CMOS technology demonstrate a successful integration of high-resolution conversion with stringent power and area constraints. Through meticulous architectural planning, digital synthesis, and physical layout optimization, the proposed ADC achieves a compact footprint of 1236.77 μm^2 and a total power consumption of 0.01931 mW, validating its suitability for low-power mixed-signal applications. Functional verification confirms reliable bit cycling and convergence behavior, while timing and leakage analyses affirm robustness under advanced process conditions. The methodology presented herein offers a scalable framework for synthesizing digitally-assisted ADCs using standard cell flows, contributing to the broader pursuit of energy-efficient data conversion in edge and embedded platforms.

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