IR-UWB RFID Circuits and Systems

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To Iris

Abstract

Radio-frequency identification (RFID) technology has been applied extensively in logistic and supply chain applications. Long-range passive RFID systems offer higher reliability and flexibility compared to conventional bar-code systems. However, limitations such as sensitivity to multipath fading and diffraction grating exist due to the narrowband technologies used. Also, industries show interest in embedding precise localization ability in such systems which is difficult to achieve using narrowband communications.

After the Federal Communications Commission released an ultra-wide bandwidth (3.1–10.6 GHz) for unlicensed use in 2002, impulse-radio (IR) ultra-wideband (UWB) communications have drawn lots of attention from both academia and industry. The large bandwidth (in other words short pulse duration) not only improves the communication quality compared to the narrowband counterparts, but also provides an excellent localization ability. This makes IR-UWB technology a potential candidate for next generation long-range passive RFID systems.

The main goal of this work is to apply UWB technology to advance the current long-range passive RFID system performance. A novel passive IR-UWB RFID system has been proposed. The potential advantages are long tag reading range with localization ability, insensitivity to surrounding environments and high security. A wireless-powered IR-UWB transmitter for the proposed system has been successfully demonstrated in a TSMC 90 nm CMOS process. Together with the coherent IR-UWB receiver implemented by the author's research group, implementations of the proposed RFID system become possible.

Moreover, the power consumption and other specifications of individual components have to be considered also in order to maximize the system performance. Research has been conducted on several functional blocks including IR-UWB pulse generator, clock generator and reference circuit. Novel topologies and solutions have been proposed and verified. Experimental results have proven competitive performance compared to other published state-of-the-art counterparts.

"*A scientific man ought to have no wishes, no affections, a mere heart of stone.*"

— Charles Robert Darwin

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"*Assume a virtue if you have it not.*"

— William Shakespeare

Contents

List of Acronyms

AoA	Angle-of-Arrival
BGR	BandGap Reference circuits
BJT	Bipolar Junction Transistor
BPSK	Bi-Phase Shift Key
BW	BandWidth
CMOS	Complementary Metal-Oxide-Semiconductor
CDMA	Code-Division Multiple Access
DC	Direct-Currernt
DL	Delay-Line
EIRP	Equivalent Isotropically Radiated Power
ETSI	European Telecommunications Standards Institute
ERP	Effective Radiated Power
FB	Fractional Bandwidth
FCC	Federal Communication Commission
FoM	Figure-of-Merit
HFWG	High-Frequency Waveform Generator
ILD	Injection-Locking frequency Divider
ISM	Industrial Scientific and Medical
IR	Impulse Radio
OOK	On-Off-Key
PD	Propagation Delay
PG	Pulse Generator
ppm	parts per million
PRF	Pulse Repetition Frequency
QF	Quality Factor
RF	Radio-Frequency
RFID	Radio-Frequency IDentification
RTL	Real Time Localization
RX	Receiver
MEMS	Micro-Electro-Mechanical System
MPC	Multi-Pulse Combination
NB	NarrowBand
SNR	Signal-to-Noise Ratio
SRD	Short-Range Device

TC	Temperature Coefficient
TSMC	Taiwan Semiconductor Manufacturing Company
TX	Transmitter
UHF	Ultra-High-Frequency
USD	United States Dollar
UWB	Ultra-WideBand
XO	CRYStal Oscillator

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"*Two things are infinite: the universe and human stupidity; and I'm not sure about the universe.*"

— Albert Einstein

Chapter 1

Introduction

1.1 Motivations

Radio-frequency identification (RFID) has been recognized as one of the most important radio innovations in the 21st century and permeates our daily life everywhere [1]. The research of RFID technology has started in 1948, but did not draw too much attention. Recently, the RFID market has experienced a tremendous growth due to improved system performance contributed by the rapid developments in integrated circuit and radio technologies [2]. A RFID market projection from 2012 to 2014 is shown in Figure 1.1. In total, around 5.9 billion tags (23% growth from 2012) were sold and the whole RFID market was worth 7.9 billion United States Dollar (USD, 13% growth from 2012) in 2013. It is expected that the

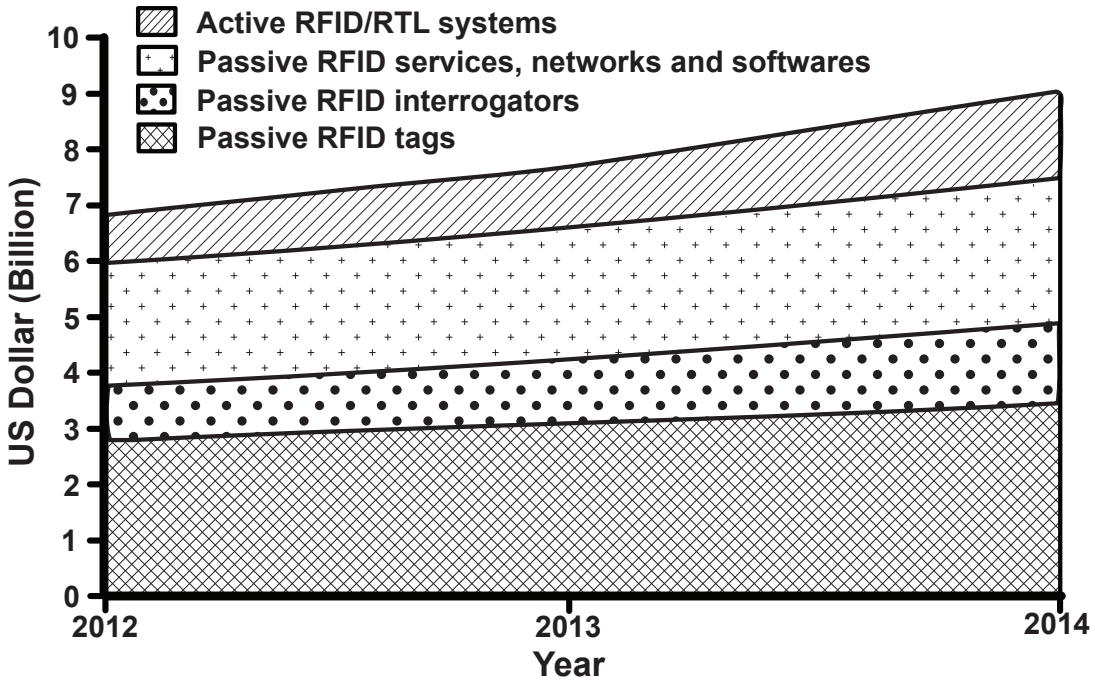

Figure 1.1: RFID market projection from 2010 to 2014 (modified from [3]).

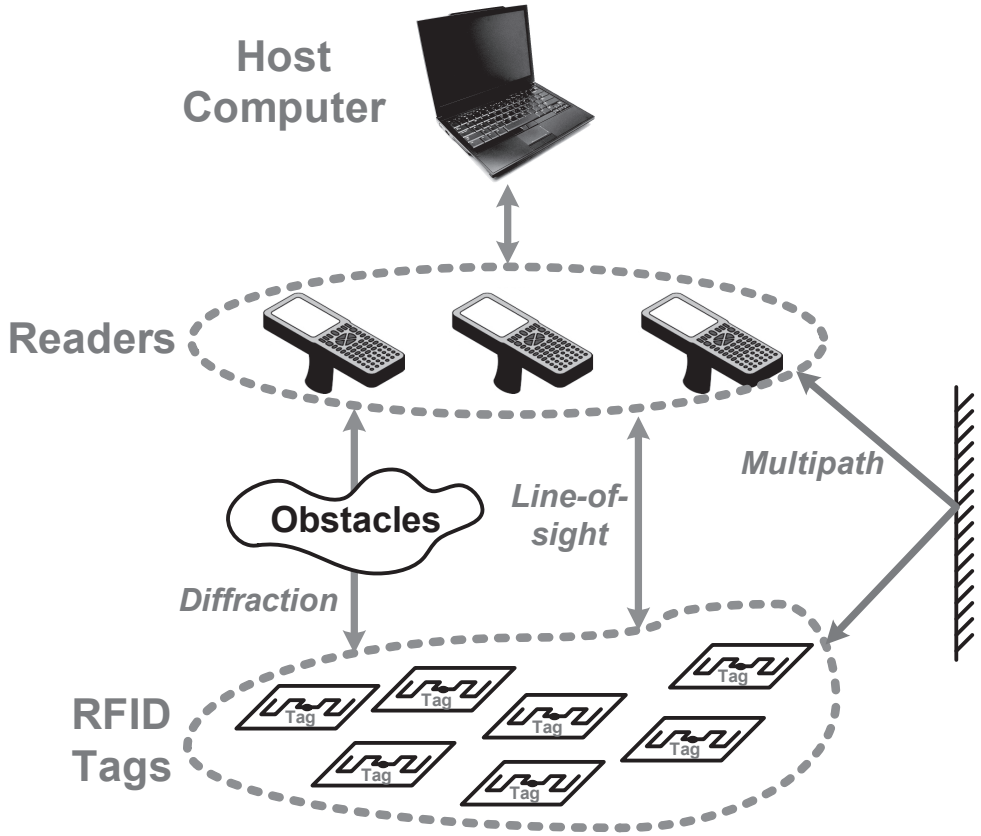

Figure 1.2: An exampled long-range passive RFID system.

RFID market will rise to 30.2 billion USD in 2024 [3], which is a huge potential market and receives significant interest from the industry.

Logistic and supply chain are the major areas of implementation for RFID technology. For example long-range passive (wireless-powered) RFID systems (with a reading range of around ten meters) have been adopted on item-tracking in large spaces like warehouses because they offer higher reliability and flexibility compared to the conventional bar-code systems with low cost (a tag can cost less than 0.1 USD nowadays). Such systems usually contain a host computer, readers and tags, which is briefly illustrated in Figure 1.2 [4]. The readers transfer energy and read/write data from/to the tags. The host computer controls and collects data from the readers depending on the targeted applications.

Although long-range passive RFID systems have been widely used in recent years, limitations are still significant because they are based on narrowband (NB) communication technologies. One of the main problems is the sensitivity to the surrounding environment since NB radios are prone to multi-path fading, diffraction grating and jamming [5]. Also, if the tags use the same frequency for energy-harvesting and communication, they may interfere with other tags and/or readers when they are too close to each others [6]. Another consideration is security (eavesdropping), data en-/decryption may not be possible due to the limited energy available on the tag side. In addition, there is interest from the industry on embedding real time localization (RTL) functions to such systems [7], however it is difficult to perform precise localization using the NB technologies [8].

After the Federal Communication Commission (FCC) of the United States released a large bandwidth (BW) for unlicensed uses in 2002 [9], impulse-radio (IR) ultra-wideband (UWB) communication has become an active research topic and provides many advantages, including high data rate and precise localization ability, over the NB counterparts. As a result, there are attempts (for example [7,10–12]) on applying the UWB technology to passive RFID applications. However, most of the purposed solutions have limited reading range (less than one meter) because of the limited energy available on the tag side and weak emission power limited by FCC.

The main goal of this work is to apply the UWB technology to advance the current long-range passive RFID technology. A novel passive IR-UWB RFID system has been proposed. The potential advantages are long tag reading range (several meters) with localization ability, insensitivity to surrounding environments and high security. A wireless-powered IR-UWB transmitter (TX) for the proposed system has been successfully demonstrated in a Taiwan Semiconductor Manufacturing Company (TSMC) 90 nm complementary metal-oxide-semiconductor (CMOS) process [13]. Together with the coherent IR-UWB receiver (RX) proposed in [14], implementations of the proposed RFID system becomes possible. Moreover, the power consumption and other specifications of individual components have to be considered also in order to maximize the system performance. Novel circuit solutions are proposed and analyzed. Experimental results have showed competitive performance compared to other published state-of-the-art counterparts.

1.2 A Brief Overview of Long-Range RFID Systems

1.2.1 Passive, Active and Semi-Passive RFID Systems

The RFID systems nowadays can be divided into three main categories by the powering schemes for the tags [15, 16], brief descriptions and their operations are listed as follows:

1. *Passive RFID systems* are the most commonly used type nowadays because no battery is required on the tag side which makes them low-cost and small-size. The signals (may include clock signal) and energy are sent from the reader with a distance up to around ten meters, for example [17] and [18]. Backscatter or load modulation is usually used for communications and channel separation is usually done by time-division multiple access [15].

2. *Active RFID systems* are essentially full radio transceiver systems and the tags are battery-powered. The battery gives the possibility of embedding more functionalities and building up more reliable and longer-range (can reach 100 meters [19]) communications. The trade-offs are increased product cost and size for the tags. Another consideration is maintenance [2,20], battery-replacement may not be easy for some applications like in-wall and harsh-environment monitoring. This increases the maintenance cost and degrades the flexibility of such tags.

3. *Semi-passive RFID systems* are a balance between systems 1 and 2. The tags contain a battery for supplying energy to the digital control circuits only. This eliminates the need for energy-harvesting, thus the reading distance is enhanced compared to the passive solutions. Meanwhile, backscatter modulation is utilized for communication, this eliminates the power-demanding radio-frequency (RF) signal transmissions and, hence, increases the battery life compared to the active solutions.

1.2.2 System-Level Specifications

1.2.2.1 Reading Range

One of the most important specifications of the RFID systems is the reading range between the tags and the readers. For long-range electromagnetic-coupling RFID systems[1], the reading range depends on several parameters and the relationship can be briefly shown by using the well-known Friis transmission equation [21]:

$$\frac{P_R}{P_T} = G_R G_T \left(\frac{\lambda}{4\pi R}\right)^2 \tag{1.1}$$

where P_R and P_T are the power available at the receiving antenna input and the output power at the transmitting antenna respectively. G_R and G_T are the antenna gains of the receiving and transmitting antennas respectively, λ is the signal wavelength, and R is the distance between the antennas. Two assumptions are made here. First, the antennas are sufficiently far away from each other and operate in far-field regions. In other words, the distance between them is larger than $\frac{2D^2}{\lambda}$, where D is the largest dimension of either antenna. Second, only the free space path loss is considered.

It can be seen from (1.1), assuming the same RX sensitivity, the reading range can be increased by:

1. *increasing the emission power P_T*. Note that the maximum emission power depends on the signal frequency and regulations of different country.

2. *increasing the antenna gains G_T and G_R* which depend on the topology and is proportional to the antenna size.

3. *reducing signal frequency, in order words increasing λ*. The available frequency bands depend on regulations of different country. Also, the antenna size is proportional to λ assuming the same gain.

[1]Short-range RFID systems usually utilize inductive- and capacitive-coupling for energy transfer and data transmissions.

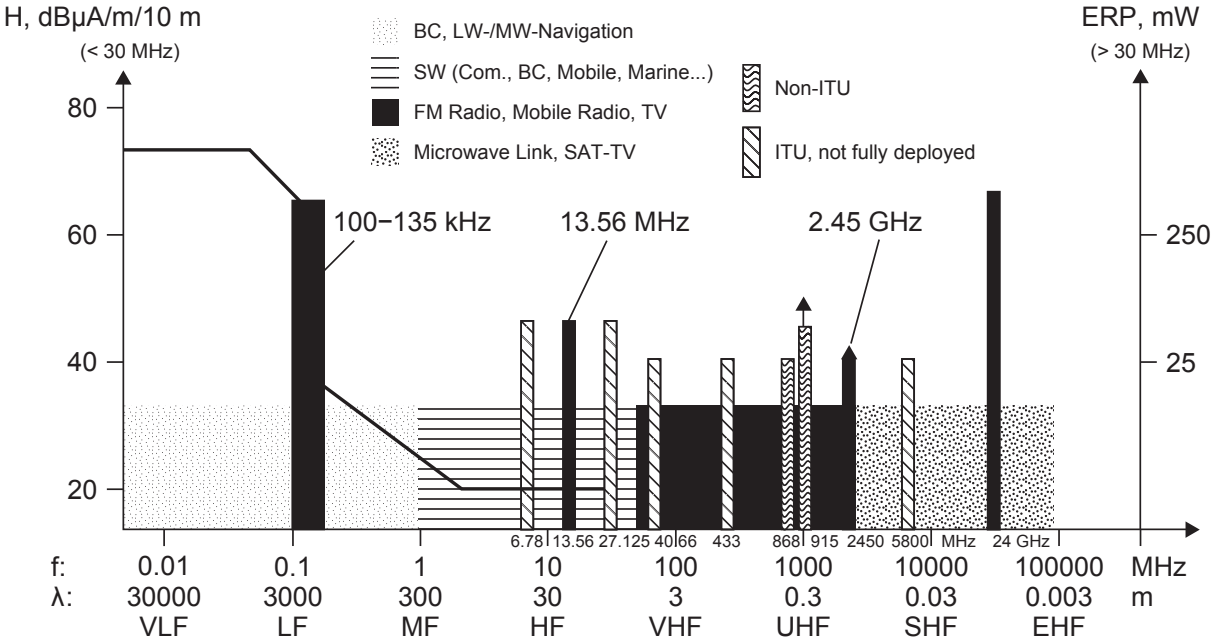

Figure 1.3: Possible RFID operating frequency ranges together with the frequency bands occupied by other radio systems (modified from [15]).

1.2.2.2 Operating Frequency

One of the very first considerations on RFID system designs is the choice of the operating frequency. In addition to the worldwide available industrial scientific and medical (ISM) bands 6.78 MHz, 13.56 MHz, 27.125 MHz, 40.68 MHz, 433 MHz, 2.4 GHz, 5.8 GHz and 24.125 GHz [15], different countries or regions have released additional frequency bands which can be used for RFID applications [15]. Most of them are located at around 900 MHz, for example the ISM band (902–928 MHz) released by FCC, the short-range device (SRD, 868–870 MHz) and RFID (865–868 MHz) bands released by the European Telecommunications Standards Institute (ETSI). For simplicity, the frequency range 865–956 MHz will be referred to as "900 MHz ultra-high-frequency (UHF) band" in this dissertation. Figure 1.3 depicts the possible operating frequency bands up to 24 GHz for RFID systems together with the frequency bands occupied by other radio systems [15]. The ISM bands provide the possibility of implementing RFID systems which can be used globally, however the interference from other radio devices operating on the same ISM band can be problematic.

The maximum emission power heavily depends on the countries and frequency bands. Two remarkable frequency bands are the 900 MHz UHF and 2.4 GHz ISM bands which provides significantly higher emission power than the other bands. In the 900 MHz UHF band, the available powers are 4 W effective isotropically radiated power (EIRP) and 2 W effective radiated power (ERP)[2] in the United States and most European countries respectively. In the 2.4 GHz ISM band, maximum 4 W ERP/EIRP is allowed to radiate in these countries. In many other countries, regulations are either similar to those of FCC or ETSI [15, 22, 23].

From (1.1), it can be found that longer wavelengths (λ) result in lower propagation losses,

[2]For purposes of comparison, 2 W ERP is equivalent to 3.2 W EIRP [22].

hence longer reading range can be obtained with a trade-off of larger antenna size. On the other hand, the penetration[3] and diffraction[4] abilities are relatively worse for shorter wavelengths. As a balance between different parameters discussed, the 900 MHz UHF band is widely adopted for long-range passive RFID systems [23]. Some commercial examples can be found in [17] and [18]. The 2.4 GHz ISM band is also preferred because of its worldwide-availability and smaller antenna size. Nevertheless the severe interferences from other radio devices may cause more complicated communication protocols and relatively large power consumption. As a result, it is more commonly used for active RFID systems.

1.2.3 Internet-of-Things and Other Applications

In the future, every single object, no matter in virtual or physical form, could have their unique identifier and communicate with other objects in an internet-like environment, the co-called internet-of-things (IoT). The concept has been addressed widely in recent years [25–27] and it is believed that 30 billion devices will be wirelessly connected to the IoT by 2020 [28]. It is expected that long-range passive RFID systems will take an important role for such applications. By embedding different kinds of sensor [29] to the passive RFID tags, useful data can be transmitted with simple circuitries and low-cost wireless solutions. Some successful examples can be found in [30–32]. Nevertheless the IoT technology development is still in early stages and related implementations are not covered in this work.

Another well-developed area is the road-toll and vehicle identification systems which traditionally require lots of manpower and resources to maintain. The 5.8 GHz ISM band is mainly utilized by these applications and some countries even allow extra emission energy compared to other radio systems [15]. In addition, interest has been shown on applying long-range passive RFID tags to track moveable items and persons such as airport baggage handling and patient tracking in hospitals [7].

1.3 An Introduction to UWB Technology

1.3.1 A Brief History of UWB Technology

UWB communication is considered as a new technology, indeed it has been invented over a century. The first successful electromagnetic wave experiment done by Heinrich Hertz in 1886 was pulse-based, so was the first radio prototype introduced by Guglielmo Marconi in 1895 [33]. The development of UWB technology continued until NB TXs with amplitude modulation became flexible in about 1915. One of the main reasons for this change was the creation of the continuous-wave oscillator, which followed the invention of the vacuum

[3]The characteristic depth of penetration is inversely proportional to $\sqrt{\omega}$ and given as $\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$, where ω is the signal angular frequency, μ and σ are the permeability and conductivity of the material respectively [21].

[4]The diffraction effect can be explained by Huygens-Fresnel principle [24]. However, this involves intensive mathematics and is not discussed in this dissertation.

triode, by Alexander Meissner in 1913 [34].

After this, UWB technology was forgotten for more than four decades. In the early 1960s, sampling oscilloscopes which required sub-nano-second baseband pulses were investigated and aided the development of the UWB field. UWB technology started to be applied on radar applications in the late 1960s [35]. Since the late 1990s, UWB technology has become more commercialized, companies such as Time Domain [36] were formed around the idea of consumer UWB radios [37, 38]. The year 2002 was a milestone of UWB technology, FCC issued a ruling that UWB technology could be used for some applications including imaging and vehicular radar. An extremely wide bandwidth (3.1–10.6 GHz) was released for unlicensed uses on most applications [9]. Since then, UWB technology has drawn lots of attention from both academic and industry. Notice that the term UWB was first introduced around 1989 by the Department of Defense of the United States [37].

UWB radios nowadays can be divided into two forms in literature, orthogonal frequency-division multiplexing and IR. The former one divides the large UWB band into several sub-bands in order to use the BW more efficiently, the latter one intends to generate very short duration impulses. IR radios provide several advantages over the NB counterparts and are focused in this work. The term IR-UWB is adopted in this dissertation to differentiate between these two forms and signify a number of synonymous terms like carrier-free, time domain, and nonsinusoidal.

1.3.2 FCC Regulations on UWB Communications

After FCC issued their rules on UWB devices, different countries started to enforce their own standards and regulations [39]. In this work, we mainly focus on utilizing the UWB band (3.1–10.6 GHz) released by FCC since it provides the largest usable BW and, hence, greatest research interest.

1.3.2.1 Definitions of UWB Signals

The following parameters are defined according to [9].

1. *UWB bandwidth* ($BW_{-10\text{dB}}$) is the frequency band bounded by the points that are 10 dB below the peak of the power spectrum. The peak frequency is designated to f_P, the upper boundary is designated f_H and the lower boundary is designated f_L. This also means

$$BW_{-10\text{dB}} = f_H - f_L \tag{1.2}$$

2. *Center frequency* (f_C) is the average of f_H and f_L, that is,

$$f_C = \frac{f_H + f_L}{2} \tag{1.3}$$

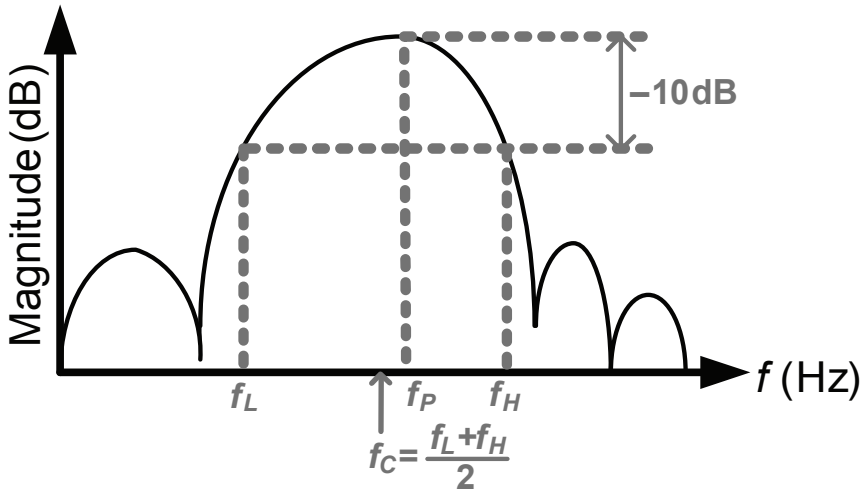

Figure 1.4: A illustration of several FCC regulation parameters.

3. *Fractional bandwidth* (FB) is defined as

$$\text{FB} = \frac{BW_{-10\text{dB}}}{f_C} = 2\frac{f_H - f_L}{f_H + f_L} \tag{1.4}$$

The situation is depicted in Figure 1.4. According to the FCC part 15 regulation [9], transmitted UWB signals need to have a FB equal to or greater than 0.2 or have a $BW_{-10\text{dB}}$ equal to or greater than 500 MHz, regardless of the FB.

1.3.2.2 Emission Energy and Spectrum Mask Regulations

FCC limits the transmitted energy of UWB devices at different frequencies so as to avoid interference with already existing NB radio systems, this can be summarized by the spectral masks depicted in Figure 1.5. The average EIRP of transmitted UWB signals is limited to be –41.3 dBm/MHz within the UWB band and even lower outside this band. Moreover, the peak power contained within a 50 MHz BW centered on f_P has to be smaller than or equal to 0 dBm EIRP, which is not shown in Figure 1.5.

1.3.3 Advantages of UWB Communications

The ultra-wide BW not only provides higher date rate, but also the possibility of reducing system power consumption. It can be proved by considering Shannon's capacity equation

$$C = BW \log_2\left(1 + \frac{P_S}{P_N}\right) \tag{1.5}$$

where C is the maximum channel capacity, P_S and P_N are the signal and noise powers respectively. Note that the channel capacity grows linearly with BW, but only logarithmically with P_S. This also implies for the same channel capacity, we can reduce P_S non-linearly and

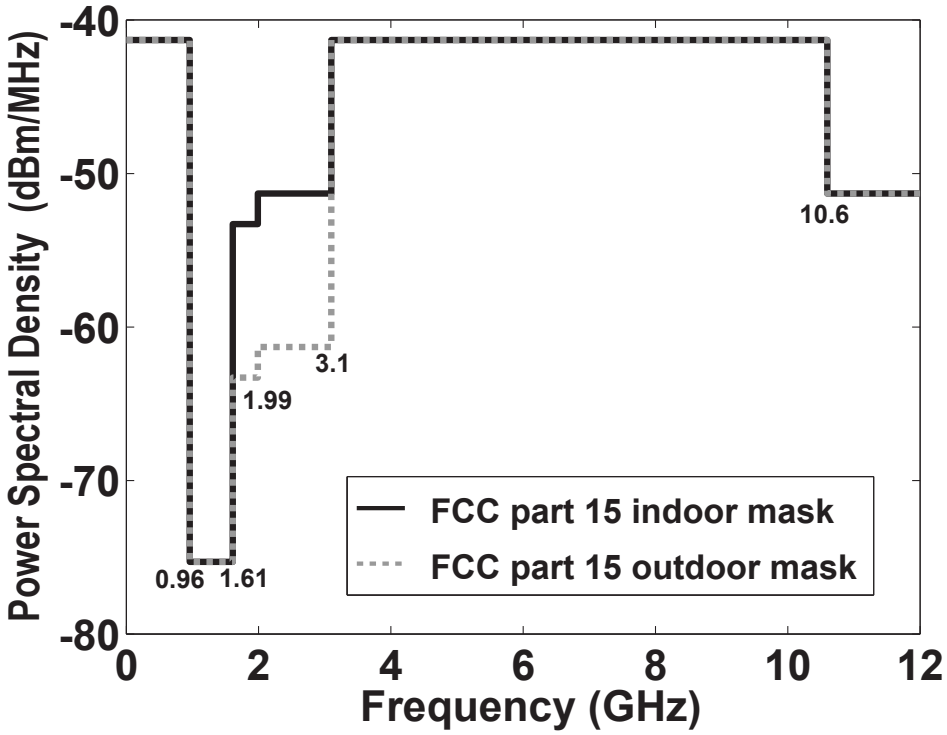

Figure 1.5: FCC part 15 indoor and outdoor masks.

significantly by increasing BW. Furthermore, IR-UWB TXs generate very short-duration impulses which may not require upconversion [38] and clock-less IR-UWB RXs have been reported [14, 40]. IR-UWB radio systems without frequency-conversion are now possible, the circuit complexity, power consumption and chip area can be reduced compared to the conventional NB counterparts.

Another advantage is the excellent localization ability contributed by the extremely short pulse width [8, 41], centimeter localization resolution has been demonstrated in [14, 42, 43]. In addition, the noise-like nature of UWB signals make them difficult for unintended users to detect and robust to eavesdropping [5].

The high temporal resolution of UWB signals results in low fading margins, implying robustness against multipath. The multipath components can also provide an excellent energy capturing capability, for example rake RXs can be implemented to lock into multipath echoes, collect energy and, hence, improve performance. Also some innovative approaches such as location fingerprinting based on the shape of channel impulse responses can be used [44]. Moreover, UWB signals are relatively insensitive to diffraction grating as they span a very wide frequency range. Nevertheless, the UWB band overlaps the frequency bands occupied by other NB radio systems with much higher power levels (for example 802.11a), attention should be paid to the interference issues [5].

1.4 Dissertation Outline

The main goal of this work is to apply the IR-UWB technology to advance the current long-range passive RFID system performance. A novel passive IR-UWB RFID system is proposed. This work focuses on the designs and implementations of the TX and related circuits. In the meantime research on RX circuit design has been conducted in the author's research group, with some results published in [14, 38]. In addition, research has been conducted on individual components like IR-UWB pulse generator (PG), reference circuit and clock generator for improved performance, especially the power consumption. Reduced power consumption of individual components can improve the sensitivity and supply noise problem of the TX.

This dissertation is written on the basis of a collection of papers. Seven papers are included and listed as follows:

[I] K. K. Lee, M. Z. Dooghabadi, H. A. Hjortland, Ø. Næss, and T. S. Lande, "A novel 6.5 pJ/pulse impulse radio pulse generator for RFID tags," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems*, Dec 2010, pp. 184–187.

[II] K. K. Lee, M. Z. Dooghabadi, H. A. Hjortland, Ø. Næss, and T. S. Lande, "A 5.2 pJ/pulse impulse radio pulse generator in 90 nm CMOS," in *Proc. IEEE International Symposium on Circuits and Systems*, May 2011, pp. 1299–1302.

[III] K. K. Lee, H. A. Hjortland, and T. S. Lande, "IR-UWB technology on next generation RFID systems," in *Proc. NORCHIP*, Nov 2011, DOI: 10.1109/NORCHP.2011.6126697.

[IV] K. K. Lee and T. S. Lande, "Analysis and design of sub-μW bandgap references in nano-meter CMOS", in *Proc. IEEE International Midwest Symposium on Circuits and Systems*, Aug 2013, pp. 93–96.

[V] K. K. Lee, T. S. Lande, and P. D. Häfliger, "A sub-μW bandgap reference circuit with an inherent curvature-compensation property," *IEEE Transactions on Circuits and Systems I: Regular Papers*, to be published, DOI: 10.1109/TCSI.2014.2340553.

[VI] K. K. Lee and T. S. Lande, "A wireless-powered IR-UWB transmitter for long-range passive RFID tags in 90 nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, to be published, DOI: 10.1109/TCSII.2014.2350292.

[VII] K. K. Lee and T. S. Lande, "A 2.8–7.5 pJ/pulse highly-flexible impulse-radio ultra-wideband pulse-generator," preparing for publication.

The following papers are published during the Ph.D. period and contain overlapping, complementing, and additional material, but are not considered part of this dissertation.

[VIII] K. K. Lee, C. Bryant, M. Törmänen, and H. Sjöland, "A 65-nm CMOS ultra-low-power LC quadrature VCO," in *Proc. NORCHIP*, Nov 2009, DOI: 10.1109/NORCHP.2009.5397805.

[IX] K. K. Lee, C. Bryant, M. Törmänen, and H. Sjöland, "Design and analysis of an ultra-low-power LC quadrature VCO," *Analog Integrated Circuits and Signal Processing*, vol. 67, no. 1, pp. 49–60, Apr 2011.

[X] K. K. Lee, Ø. Næss, and T. S. Lande, "A 3.9 pJ/pulse differential IR-UWB pulse generator in 90 nm CMOS," in *Proc. Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*, Oct 2011, pp. 115–118.

[XI] K. K. Lee and T. S. Lande, "Co-design of antenna, matching network and voltage rectifier in state-of-the-art CMOS," in *Proc. IEEE International Midwest Symposium on Circuits and Systems*, Aug 2012, pp. 49–52.

[XII] K. K. Lee, K. Granhaug, and N. Andersen, "A study of low-power crystal oscillator design," in *Proc. NORCHIP*, Nov 2013, DOI: 10.1109/NORCHIP.2013.6702036.

[XIII] M. Z. Dooghabadi, H. A. Hjortland, Ø. Næss, K. K. Lee, and T. S. Lande, "An IR-UWB transmitter for ranging systems", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol: 60, no: 11, pp. 721–725, Nov 2013.

This dissertation is organized as follows: Chapter 2 describes the work done by the author in the papers [I–VII] and provides background of the related work in literature. Chapter 3 concludes with a brief summary of the work and a discussion of future research directions. The technical papers are enclosed in the appendix section.

"*Solitude is painful when one is young, but delightful when one is more mature.*"

— Albert Einstein

"*I love to be alone. I never found the companion that was so companionable as solitude.*"

— Henry David Thoreau

Chapter 2

Work Descriptions

This chapter is a guideline for reading papers [I–VII]. The papers can be divided into four main topics: IR-UWB RFID systems, IR-UWB PGs, clock generators and reference circuits. They will be discussed individually in each subsection. Research background and main contributions by the author are presented.

2.1 IR-UWB RFID Systems

2.1.1 Background

Active IR-UWB RFID systems (including battery-powered IR-UWB transceivers) have been developed and showed very promising results (for example [45–50]). In [45], a communication distance of 200 meters with a maximum error of 15 cm has been achieved. The localization error has even been shown to be as low as 1 cm in [43]. Nevertheless active RFID tags (or the transceiver modules) and batteries are rather expensive (>10 USD) for logistic and supply chain applications. As a balance between the battery lifetime and system performance, a semi-passive IR-UWB RFID system has been proposed in [7] and [51]. The communication is performed by UWB backscattering modulations with a UHF signal (around 900 MHz) wake up. Nevertheless active and semi-passive solutions require battery replacement which makes them not suitable for some applications.

Passive IR-UWB RFID systems (or wireless-powered IR-UWB transceivers) have been reported in [10–12,52–55]. One of the main challenges of wireless-powered IR-UWB radio systems [10–12,52] is to harvest enough energy for data transmissions. The energy-consumption of state-of-the-art IR-UWB PGs is in the order of 10 pJ/pulse [56–60], which corresponds to 100 μW with a 10 MHz pulse repetition frequency (PRF), and the efficiency of state-of-the-art far-field RF voltage rectifiers is around 20–30% [61–64]. If we assume that the rectifier efficiency is 25% and an ideal matching network is added such that its insertion loss and the reflection loss can be eliminated, the system minimum input power is 400 μW ($\approx$–4 dBm) which corresponds a wireless energy transmission distance of approximately three meters by

using (1.1) (Friis transmission equation) with 900 MHz 4 W EIRP radiation and 0 dB gain transmitting/receiving antennas. The power consumption from the other functional blocks and other nonidealities further decrease the distance to less than one meter [10, 52].

To increase the energy transmission distance, a multi-mode operation scheme has been adopted in [11, 12, 31] with a potential trade-off of more complicated hand-shake protocols. The idea is to introduce an energy-harvesting mode, only a voltage sensor and related circuits are enabled to minimize the system power consumption (in the order of μW) during this period. A storage capacitor is charged up and other circuits are enabled when enough energy is harvested. An energy transmission distance of 15.7 meters has been reported in [12]. Nevertheless the communication distance of wireless-powered RFID systems is still unsatisfied due to the limited energy available and, hence, weak emission power on the TX side [11, 12]. Notice that the storing energy is given as $\frac{1}{2}C_S V_{DD}^2$, where V_{DD} and C_S are the supply voltage and capacitance of the storage capacitor respectively. The storing energy could be increased by using a larger storage capacitor, however this also increases the leakage current and charging time. The long charging time may degrade the system capacity performance. In [11, 12, 31], C_S ranges from 4 to 211 nF, the storing energy is still limited.

Very interesting chip-less IR-UWB solutions[1] (without integrated circuits) have been proposed [32, 53–55, 67] to further reduce the production cost. The idea is to connect a UWB antenna to different transmission line networks, the backscattered pulses are varied correspondingly and can be used for identifications. The trade-offs are relatively shorter reading range [55] and limited functionalities due to the lack of energy sources on the tags.

2.1.2 Related Work and Contributions

Published wireless-powered IR-UWB tags in literature [10–12, 52] offer limited reading range due to the reasons aforementioned. To improve this, the multi-mode operation scheme is adopted and the tag data is transmitted repeatedly, this introduces higher processing gain and averages out the noise. As a result, the signal-to-noise ratio (SNR) and, hence, reading range are increased. Nevertheless the hand-shake protocols become complicated when there are large number of tags and amount of data in the system. This may increase the tag circuit complexity and energy consumption. To solve this, a long-range passive IR-UWB RFID system using a uni-directional communication scheme has been proposed in [III] and slightly modified in [VI]. The channel separation is given by the system asynchronous code-division multiple access (CDMA) and inherent ALOHA properties. Every tag requires different time to harvest energy due to process variation, component mismatch and distance to the readers, transmissions will be sufficiently distributed for acceptable interference, even with a large number of tags in operation.

A wireless-powered CDMA IR-UWB TX for the proposed RFID system has been presented in [VI]. The TX is wireless-powered by a 900 MHz UHF signal and starts transmissions of symbols containing 128-b PN codes when enough energy is harvested. On-off-key

[1] Chipless RFID solutions are used on NB RFID systems also, more details can be found in [65] and [66].

(OOK) modulation is adopted because of the simple structure and low energy consumption of OOK PGs, although bi-phase shift key (BPSK) modulation could provide better communication quality [68]. System co-designs of different building blocks are proposed to improve tags performance without additional power consumption overhead. A proof-of-concept prototype has been successfully implemented in the TSMC 90 nm CMOS process. Together with elaborate RX design (an exampled structure can be found in [14]), the proposed RFID system can provide precise RTL ability. Only localization techniques which do not require synchronization between readers and tags can be used to locate the tags. The angle-of-arrival (AoA) approach is chosen as an example. Considering a reader containing an antenna array with known geometry, the AoA is estimated from the differences in arrival times for the tag transmitted signal at each of the antennas. As a result, a radial line can be formed from the reader to the tag. Precise localization can be performed by using multiple readers and intersecting the resultant radial lines. Other localization techniques and trade-offs can be found in [37, 68, 69].

2.2 IR-UWB PGs

2.2.1 Background

One of the most important components inside IR-UWB TXs is the PG. It is usually the most power-demanding component and the communication distance is greatly related to its emission energy. At the same time the emitted signal has to meet the spectrum regulation of different country to avoid interfering with other radio systems.

The basic idea of most published IR-UWB PGs is to use a high-frequency waveform generator (HFWG), which can be an oscillator, phase-locked loop or delay-line (DL), and shape its output signal to generate the desired envelope by mainly three approaches: spectrum mixing [46, 47, 49, 56, 70–72], filtering [11, 57, 58, 73–75] or multi-pulse combination (MPC) [59, 60, 76–79]. The spectrum mixing approach consists of a local oscillator and a mixer like conventional NB TXs, the high-frequency oscillator output is then mixed with the envelope shape [46, 47, 49, 70]. The power consumption and area are relatively large because more components are needed compared to the other two approaches. Moreover, the leakage from the oscillator to the antenna could be problematic. However, it is the one of the very few PG topologies that can generate high-quality BPSK IR-UWB signals. The mixing function could also be performed by switching the oscillator on and off [56, 71, 72], this eliminates the need of the mixer with a drawback of disability of generating BPSK signals.

For the filtering approach, the HFWG output signal is coupled to and filtered by a pulse shaping filter so that the resultant signal can meet the spectrum mask regulations. In additional to the circuit simplicity, another advantage is that the output parasitic capacitance, which is usually the dominating one inside the PG, can be used as part of the filter and tuned-out by inductors inside the filter. In other words, the capacitive and switching losses could be reduced. However, the filtered out-of-band energy is wasted and on-chip spiral inductors

are area-demanding.

MPC IR-UWB PGs usually utilize DLs as the HFWG. Based on the propagation delay (PD) of the DL and output drivers with different strength, Gaussian-approximate waveforms can be obtained. The MPC approach is shown to be very energy-efficient (2.5 pJ/pulse has been reported in [59]) and small-size because it contains mainly digital gates. Nevertheless most of the MPC IR-UWB PGs operate at the lower frequencies of the UWB band, this is because the capacitive and switching losses due to the output parasitic capacitance increase with frequency. Also, it is not easy to control the envelope and center frequency accurately due to process variations, filtering and/or calibration may be required. Note that for some MPC IR-UWB PGs [59, 76–78], the direct-currernt (DC) output voltage of output drivers is biased by the transistor leakage current which is usually not accurately modeled, this may increase the design difficulty.

2.2.2 Related Work and Contributions

In [I], a low-power DL-based MPC OOK IR-UWB PG structure (will be referred to as PG-I) which utilizes loose-triangular waveforms to construct a Gaussian envelope has been proposed. An acceptable spectral filling is achieved with simple circuit solutions. PG-I has been successfully implemented in a TSMC 90 nm CMOS process in [II]. Because it contains mainly digital gates, low energy consumption and chip area are obtained. A resistive divider is used to bias the DC output voltage instead of the leakage current solution adopted in [59] and [76], this can control the variation of the DC output voltage better. However, the energy consumption increases when the PRF decreases because of the static current drawn by the resistive divider. To solve this, a dynamic pre-charge scheme which turns on the resistive divider a short time before transmissions has been proposed in [II]. PG-I has been adopted in an IR-UWB TX for ranging systems presented in [XIII] and [14]. The presented TX could also be applied to active and semi-passive IR-UWB RFID systems. Note that there are differences between the post-layout simulation results in [I] and measurement results in [II], this is because the envelope and center frequency of the PG output signal are sensitive to the PD variation of the DL. Other possible reasons are the inaccuracies of the layout parasitic component extraction tools and the transistor models provided by the vendor.

Another DL-based MPC OOK IR-UWB PG structure (will be referred to as PG-II) has been proposed in [VI]. It uses an on-chip spiral inductor to tune out the output parasitic capacitance, the driving requirement and, hence, the transistor size of the output drivers are reduced. In other words, the capacitive and switching losses are also reduced which makes PG-II energy-efficient. Also, energy is concentrated at around the resonating frequency of the LC tank because of the its bandpass property, this makes PG-II less sensitive to the mismatch and temperature variation. The inductor connects the PG output to the supply voltage at low frequencies which provides electrostatic discharge protection. PG-II has been used in the wireless-powered IR-UWB TX presented in [VI].

Because of the TX multi-mode operations and limited number of pad counts, some important specifications of PG-II have not been measured in [VI]. In [VII], an improved version

of PG-II with higher flexibility (will be referred to as PG-III) has been proposed. In addition, detailed measurement results, qualitative frequency-domain and transient analyses are presented. A new figure-of-merit (FoM) has been proposed to compare different IR-UWB PGs in a more precise way. Both PG-I and PG-III show competitive performance compared to other published state-of-the-art IR-UWB PGs [VII].

2.3 Clock Generators

2.3.1 Background

Crystal oscillators (XO) are used extensively in modern radio systems. It can generate very precise and stable reference clock signals because of the extremely high quality factor (QF, in the order of 100,000) of the crystal resonators [80, 81]. Normal XOs can provide frequency stability in the order of 10 parts per million (ppm) over a wide temperature range, this can even be improved to 0.05 ppm with analog temperature compensation [82]. However, the maximum fundamental oscillating frequency is up to around 30 MHz only [83]. Micro-electro-mechanical systems (MEMS) resonators have been proposed [84] and the maximum fundamental oscillating frequency is increased to the GHz range with a trade-off of lower QF (in the order of 1,000) [82, 85]. The smaller size of the MEMS resonators [86, 87] also enables the possibility of embedding the whole front-end in a single package (the so-called system-in-package solution) for improved performance. Note that the oscillator power consumption is inversely proportional to the resonator QF, on the other hand the start-up time is exponentially proportional to the resonator QF [XII]. The long start-up time may limit the usability of crystal/MEMS oscillators on IR-UWB TXs which are usually turned on and off from time to time.

Ring oscillators are possible candidates for passive RFID systems [88] because of their simplicity and energy efficiency. However, the output frequency varies with temperature, this may limit the system operating temperature range. Temperature-compensated ring oscillators have been proposed to reduce the frequency variation (can be less than 1% over a temperature range of 100°C [89–91]) with slightly increased complexity. Nevertheless the output frequency error due to process variations can be as large as ±20%, post digital signal processing [92] and/or trimming may be required.

Very accurate chip-rate is usually required for CDMA systems. A possible low-power solution for wireless-powered radio systems is to lock to the input RF signals with simple circuitries. A clock recovery solution using a digital frequency-locked loop has been proposed in [93] for Electronic Product Code[2] generation-2 RFID tags [94]. Injection-locking solutions have been proposed in [11, 30, 95–98]. They provide lower circuit complexity, faster start-up time (including locking time) and, thus, better energy efficiency compared to the clock recovery solution. However, for most injection-locking frequency dividers (ILD) for RFID applications, the injection input generates a resistive load to the antenna which induces losses

[2]Electronic Product Code provides well-accepted RFID standards and data structures.

and degrades the system sensitivity.

2.3.2 Related Work and Contributions

The injection-locking approach is adopted for the proposed IR-UWB RFID system because of the high energy-efficiency advantage. If the targeted output frequency is close to the ILD free-running oscillating frequency, the start-up time (including lock time) can be very short (a few clock cycles according to simulations). A novel ILD co-designed with RF voltage rectifier has been proposed in [VI]. It is based on the structure proposed in [99]. Unlike other ILDs for RFID applications [11, 30, 95], the DC voltage of the injection input is biased by either resistors or diode-connected transistors which generate resistive loads to the antenna and degrade the sensitivity, the proposed ILD co-designs with the RF voltage rectifier and introduces only a small capacitive load to the antenna. As a result, this reduces the resistive loss and the system sensitivity is improved. The proposed ILD has been successfully implemented in the TSMC 90 nm CMOS process and adopted in the wireless-powered IR-UWB TX presented in [VI].

2.4 Reference Circuits

2.4.1 Background

Bandgap reference circuits (BGR) generate precise reference signals which are insensitive to process, voltage and temperature variations, and have been used for decades because of their reliability. However, very low power consumption (sub-μW or even lower) is needed for the wireless-powered applications [30, 100], large resistance is needed in order to achieve this. This can increase the chip area substansiously. As a result, only a few sub-μW BGRs can be found in literature [30, 101, 102]. Some research has been conducted on CMOS-only reference circuits which generate the output voltage based on CMOS transistor threshold voltage [103–105] or its difference [106, 107]. Nevertheless, design trade-offs such as sensitivity to process variations, precision and flexibility have to be considered also.

The minimum width of resistors scales down with the continuing aggressive development of CMOS technology. Mega-ohm resistors can now be realized with a reasonable area in state-of-the-art CMOS processes, hence sub-μW BGR power consumption is now possible. For example the high-resistance poly resistor without salicide in the TSMC 90 nm CMOS process, its resistivity can be as large as 0.16 MΩ per 100 μm^2 and would increase even more favorably with more modern technology nodes. The resistor area is now less dominating, and becomes comparable to other components for BGR design.

Another important BGR design parameter is the temperature coefficient (TC). For CMOS BGRs, this non-ideality is mainly due to the high-order temperature dependence of bipolar junction transistor (BJT) base-emitter voltage [108–110]. Different temperature compensation techniques have been developed [111–122], most of them require additional components

and power consumption. A remarkable exception is [121], the BGR high-order temperature dependence is compensated by incorporating two different types of resistor whose first-order TCs are of opposite sign. Nevertheless intensive trimming may be needed to match the resistor ratios because the resistors are with different types. More curvature-compensation techniques and related discussion can be found in [123].

2.4.2 Related Work and Contributions

An analysis of ultra-low-power BGR designs in nm CMOS processes has been presented in [IV]. Three different widely-used BGR topologies have been studied. One of them (will be referred to as BGR-I) is very interesting with limited results reported. To get more insight, BGR-I has been implemented in the TSMC 90 nm CMOS process and verified. BGR-I has been used in the wireless-powered IR-UWB TX presented in [VI].

A detailed discussion between resistor-based BGRs and CMOS-only reference circuits and different design considerations of ultra-low-power BGRs in nm CMOS processes have been presented in [V]. In addition, a new current-mode BGR topology with an inherent curvature-compensation property (will be referred to as BGR-II) has been presented. The proposed curvature-compensation technique utilizes the exponential behavior of sub-threshold CMOS transistors to compensate the BJT base-emitter voltage high-order temperature dependence and improves the TC performance. The proposed curvature-compensation technique is simple and requires no additional current consumption. Also, BGR-II is capable of generating sub-1-V output voltage and has the lowest theoretical minimum current consumption among published current-mode BGRs. BGR-II has been successfully demonstrated in the TSMC 90 nm CMOS process.

"*Worry does not empty tomorrow of its sorrow, it empties today of its strength.*"

— Corrie ten Boom

Chapter 3

Summary and Future Work

3.1 Summary

A novel long-range passive IR-UWB RFID system intended to advance the current RFID technology has been proposed in [III] and [VI]. The potential advantages are a long reading range with localization ability, insensitivity to surrounding environments and high security. In [VI], a wireless-powered CDMA IR-UWB TX intended for the proposed RFID system has been implemented in the TSMC 90 nm CMOS process and presented. Moreover, novel IR-UWB PG (PG-II), ILD and co-design schemes have been proposed to improve the TX performance with minimal power consumption overheads. The proposed RFID tag provides sufficient bandwidth for potential resolution in the centimeter range. Notice that the reader side has not been implemented due to the limited resources and time, demonstrations of the system performance require experimental verifications. Although high-precision long-range localizations have been demonstrated in [42], interference and practical limitations will probably limit localization performance in real scenarios.

In addition, several functional blocks for low-power IR-UWB radio systems have been proposed and analyzed. A OOK IR-UWB PG (PG-I) has been proposed in [I] and demonstrated in [II]. It is energy-efficient and small-size because it contains mainly digital gate. PG-I has been adopted in an IR-UWB TX for ranging systems presented in [XIII]. In [VII], a low-power highly-flexible IR-UWB PG (PG-III, which is an improved version of PG-II) has been presented. The output power, PW and center frequency are controllable. Qualitative frequency-domain and transient analyses have been presented. A new FoM has been proposed to compare different IR-UWB PGs in a more precise way. Both PG-I and PG-III show competitive performance compared to other published state-of-the-art IR-UWB PGs as shown in [VII].

In [IV], an analysis of ultra-low-power BGR designs in nm CMOS processes has been presented, a BGR topology with limited results reported in literature (BGR-I) has been fabricated to get more insight. A detailed discussion between resistor-based BGRs and CMOS-only reference circuits and different design considerations of ultra-low-power BGRs in state-of-the-art nm CMOS processes have been presented in [V]. Also, a sub-μW BGR with an

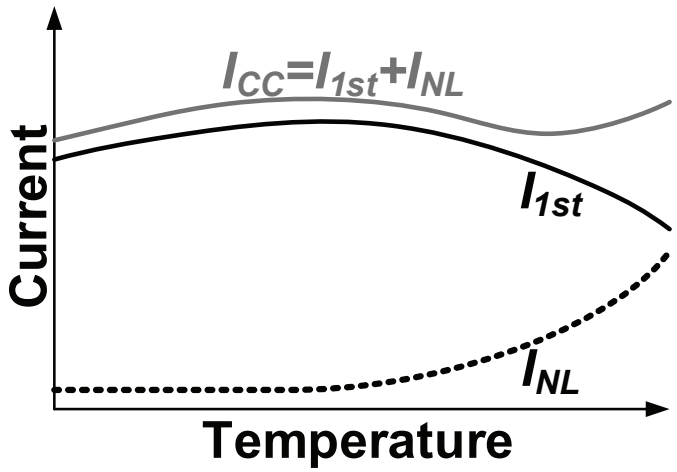

Figure 3.1: An idea of piecewise-linear curvature-compensation.

inherent curvature-compensation property (BGR-II) has been proposed and shown competitive results with other state-of-the-art voltage reference circuits.

3.2 Recommendations for Future Work

Full System Demonstrations

Although individual IR-UWB TX and RX for the proposed RFID system have been proposed in this work and [14] respectively, the full system has not been demonstrated yet because of the reasons aforementioned. Additional reader and control circuits are required. Furthermore, localization techniques like AoA and time-difference-of-arrival [37, 68, 69, 124] and control algorithms are required for RTL applications. Additional research on signal processings is needed for optimizing the system performance.

Implementations of BGR-II with piecewise-linear curvature-compensation and/or trimming.

Piecewise-linear curvature-compensation technique has been widely used on current-mode BGR designs [115–119] to extend the operating temperature range and, thus, reduce the TC. The idea is shown in Figure 3.1. The output current of a first-order BGR (I_{1st}) is summed with non-linear current (I_{NL}) which can be generated with simple CMOS circuits, the resultant current (I_{CC}) is second-order (or even higher-order) curvature-compensated. More details can be found in [125]. It may be possible to apply such technique to BGR-II for improved performance. In addition, the unwanted effects due to process variations can be minimized by trimming the resistor ratios [118, 121], this can improve both the TC and output variation performance which may be preferred for high-precision applications. The trade-offs are increased chip area, cost and testing time.

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Appendix A

Technical Paper Collection

A.1 Paper-I

K. K. Lee, M. Z. Dooghabadi, H. A. Hjortland, Ø. Næss and T. S. Lande, "A novel 6.5 pJ/pulse impulse radio pulse generator for RFID tags," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems*, Dec 2010, pp. 184–187.

A Novel 6.5 pJ/Pulse Impulse Radio Pulse Generator for RFID Tags

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***Abstract*—A novel impulse radio (IR) ultra wideband (UWB) pulse generator (PG) intended for RFID tags is presented. A new pulse-shaping approach suited for CMOS implementation is proposed. The power consumption and chip area are reduced compared to the conventional higher order Gaussian PGs. The proposed PG uses digital gates for timing achieving good power efficiency and, meanwhile, acceptable spectral filling. The circuit is scalable both in bandwidth and center frequency. The PG is designed in a TSMC 90 nm CMOS technology. Post-layout simulations show a worst-case power consumption from a 1.2 V supply to be 6.5 pJ/pulse for a 100 MHz pulse repetition frequency (PRF). The chip area is 0.00079 mm^2 (38.2 µm $\times$ 20.8 µm) for the PG core.**

***Index Terms*—IR, UWB, RFID, CMOS, Pulse generator**

I. Introduction

Viable communication solutions have been pursued actively after the Federal Communication Commission (FCC) released a large UWB spectral mask (i.e. 3.1–10.6 GHz) for unlicensed use. Most available UWB technology is based on multi-band (OFDM) solutions for proper UWB spectral filling. Today we still do not find widespread use of UWB solutions.

Another immature technology is RFID tags. Most RFID tags nowadays are using narrowband technology and powered by a battery (or inductive coupling for short-range communication). The battery increases the production cost and the tag size significantly. One noticeable exception is a single-chip RFID tag solution from Tagent [1] with on-chip energy-harvesting circuits and a 6.7 GHz UWB transmitter. The power-harvesting technology is using a 5.8 GHz carrier and limited to one meter distance indicating power-limitations in the tag.

As a first step towards green (no battery) RFID tags, we are exploring a simple and very power-efficient IR-UWB PG, which is often the most power-comsuming component of the transmitter, suitable for implementation in standard digital technology (CMOS). Unlike narrowband counterparts, IR-UWB PGs do not require precise carrier generators and the wideband transmission does not require accurate inter-pulse timing.

In this paper, a new pulse-shaping approach which requires only digital gates is proposed. The proposed pulse generator uses only digital gates for timing achieving good power efficiency and acceptable spectral filling. The circuit is scalable both in bandwidth (BW_{-10dB}) and center frequency (f_{center}) and is well suited for nanometer CMOS technology. The PG performs very well, especially in term of power consumption and chip area, and is competitive to other recently published UWB PGs [2]–[5]. Post-layout simulations show a worst-case power consumption to be 6.5 pJ/pulse for a 100 MHz PRF. In these extremely power-limited applications, leakage current must also be accounted for, hence the gate area should be kept small.

II. Pulse-Shape Generation

Higher order Gaussian pulse-shapes are widely used in IR-UWB PGs to minimize the sideband interference, however, it is hard to generate higher order Gaussian pulses in standard CMOS processes with simple circuit solutions. A piecewise Gaussian approximation (PGA) approach was proposed in [6] and a promising low-power (5.6 pJ/pulse) IR-UWB PG using a similar approach was reported in [2]. The weakness is the circuit complexity, the number of generator stages and output drivers are proportional to the order of the Gaussian function. Only one output driver is used during each phase, the un-used output drivers add output capacitance and, hence, increase the power consumption. Also, in order to adopt to international spectral regulations (band group 6, i.e. 7.7–8.7 GHz, is the only band available worldwide [7]), a high-order Gaussian derivative (15-th) is required, but not feasible due to increased parasitic capacitance.

Instead of generating higher order Gaussian waveforms, we are proposing to use several simple pulses to construct a first order Gaussian envelope. BW_{-10dB} is then determined by the envelope width and f_{center} is determined by the frequency of the generated pulses. The somehow crude generated pulses will not add significant sideband interference as long as the pulse frequency is significantly higher than the envelope frequency. The idea is depicted in Fig. 1. The amplitudes of 5 GHz triangular and sine waveforms are shaped to make a Gaussian envelope with $\alpha = 0.6$ ns. The frequency spectra are shown in Fig. 1c.

Loose-triangular pulses are selected because they can be generated easily in CMOS processes by charging and discharging a parasitic capacitor. It is difficult to model loose-triangular waveforms in mathematical simulators, however, its frequency spectrum should be somehow in between the spectra shown in Fig. 1c. f_{center} may be limited to be 5 GHz in this paper because of the technology limitations. We are expecting

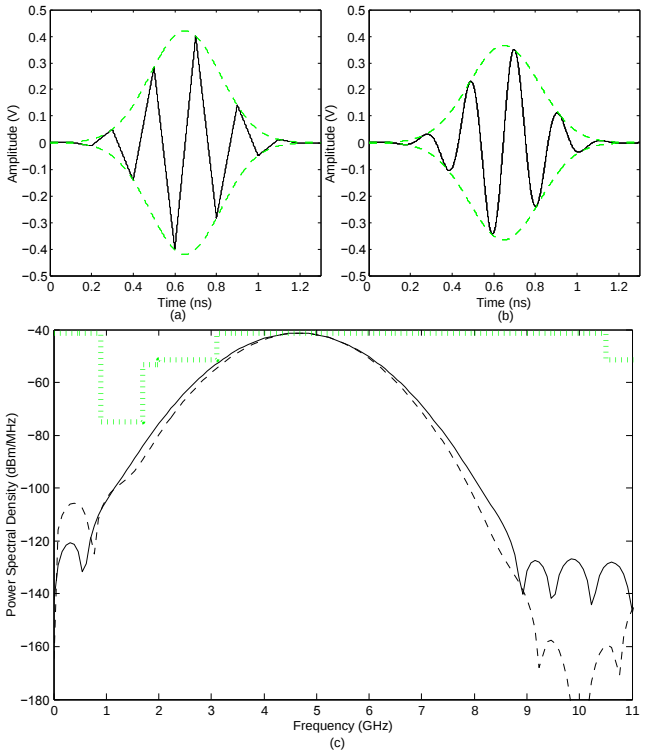

Fig. 1. (a and b) Proposed pulse-shape generation approaches (c) Dashed: Frequency spectrum of (a); Solid: Frequency spectrum of (b); Dotted: FCC mask.

it can be pushed to higher frequencies, hence better spectral utilization can be achieved with faster CMOS technology. The main advantage of this approach is its simplicity and technology scalability combined with power efficiency.

III. Circuit Implementation

Because the gate count is proportional to the number of triangular pulses generated, the weak pulses at the beginning and at the end of the pulse-sequence are omitted in order to simplify the circuit and minimize the power consumption. The resulting waveform and spectrum is shown in Fig. 2. The f_{center} is 4.8 GHz with a BW_{-10dB} of 3 GHz. Some low-frequency sidebands are observed. However, simulations show that the mismatch between the charging and discharging time is the main reason for low-frequency sidebands and omission of the weak pulses will not have a significant impact on the sidebands. The low-frequency sidebands may be reduced by adding high-pass filters, or even just exploring the antenna band-pass property.

The schematic of the proposed PG is depicted in Fig. 3. The structure is similar to the PGA-PG in [2], but the idea is different. The proposed PG contains only simple digital gates and does not have any Gaussian pulse generators. The one-shot circuit is triggered by a falling edge and creates a fixed-width pulse, τ, for each input edge. Pulse stretchers [8] are added to adjust the width of the pulses in order to minimize the sideband energy. High threshold transistors are used for the delay line to minimize the leakage current.

As mentioned, in PGA-PGs, only one output driver is on in a single phase, the un-used output drivers add undesired output capacitance and degrade the circuit performance. In the proposed PG, only loose-triangular waveforms are generated, this makes it possible to share the output drivers like the timing diagram shown in Fig. 3. One or more output drivers with different strength are combined for desired charging and discharging strength, which is a very important feature for generating multi-cycles IR-UWB pulses. The firing control logic is required for correct firing sequence. We can see that the PG contains only digital gates for timing exploring inherent gate-delays, which is very beneficial for modern CMOS technology.

IV. Layout

The layout is shown in Fig. 4. Since the PG contains only digital gates, we use only 0.00079 mm^2 silicon area. The delay line is one of the critical components in the PG and must be designed carefully for minimal mismatch. Using multiple fingers devices and sharing the drain connections may reduce the parasitic drain-capacitance. However, this may give a very long diffusion and the "Length of Diffusion" effect [9] may degrade the delay line speed. Power distribution must also be balanced and decoupled locally since gates are rail referred. Just minor drops in power supply can affect inverter delays significantly.

V. Post-Layout Simulation Results

The PG testbench is shown in Fig. 5. The 100 fF and 10 µF capacitors are the pad parasitic capacitor and coupling capacitor respectively. The 1 nH inductor accounts for the bond-wire parasitic inductance. The antenna is modeled as a 50 Ω resistive load. C_L is the loading capacitance due to the off-chip components (package, PCB and so on).

Fig. 6 shows the frequency spectra of the PG output (observed at V_{ANT}) with different C_L at the typical design corner. With 1 pF C_L, the peak is –41.9 dBm/MHz at around 4.3 GHz. The f_{center} is lower than the predicted because of the unexpected large parasitic capacitance of the delay line. The BW_{-10dB} is 2.9 GHz, which is very close to the predicted value. When C_L increases, the amplitude of triangular pulses

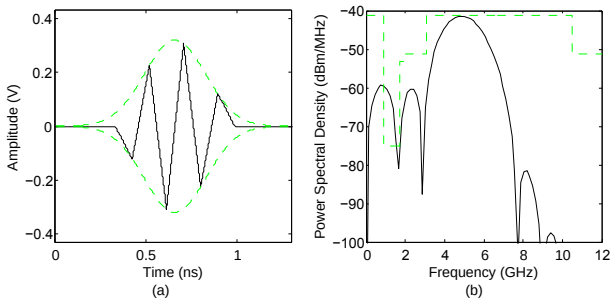

Fig. 2. (a) Adopted pulse-shape, (b) Solid: Its frequency spectrum; Dashed: FCC mask.

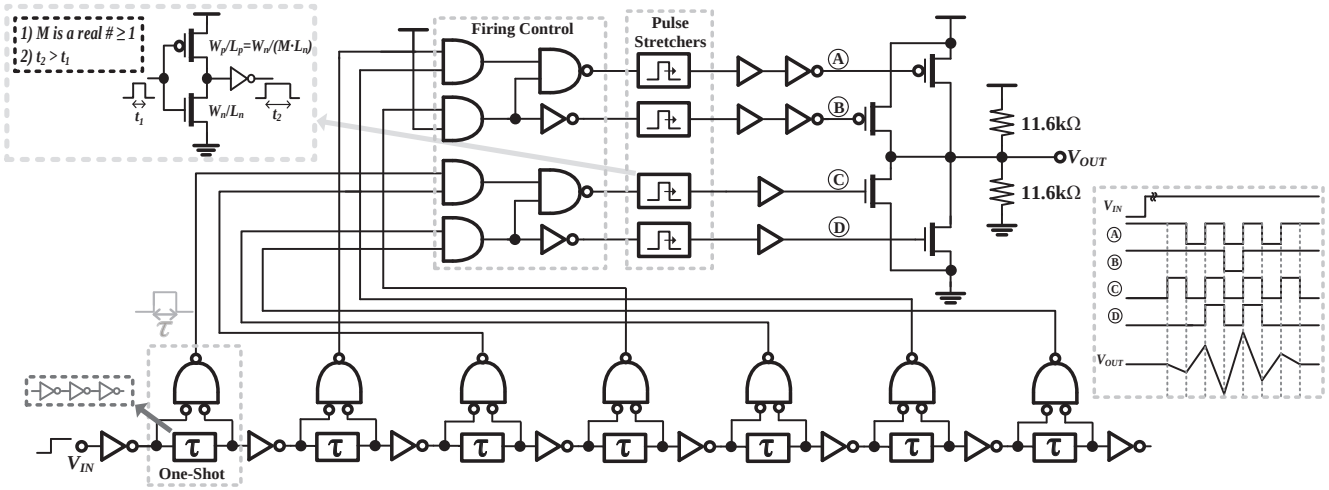

Fig. 3. Proposed PG.

decreases, which also decreases the peak of the spectra, the PG can meet the FCC requirements when C_L is larger than 1.5 pF assuming a high-pass filter added. With faster CMOS technology, we can push f_{center} to higher frequencies and achieve better spectral utilization

Fig. 7 shows a transient simulation with 2 pF C_L at the typical design corner. The pulse width (τ_{OUT}) is about 688 ps, and 820 ps for the worst case (i.e. the slow design corner). The ringing is caused by the bond-wire inductance. The power consumption from a 1.2 V supply is 6.3 pJ/pulse for a 100 MHz PRF, and 6.5 pJ/pulse for the worst case. It can be seen in Fig. 7 that the maximum PRF can be larger than 200 MHz. The frequency spectra of the PG output (observed at V_{ANT}) with 2 pF C_L at different design corners are depicted in Fig. 8.

A summary of the simulation results and a comparison to recently published IR-UWB PGs [2]–[5] are shown in Table I. The simulations show that the designed PG performs very well, especially in terms of power dissipation and area, and is competitive to the state-of-the-art IR-UWB PGs.

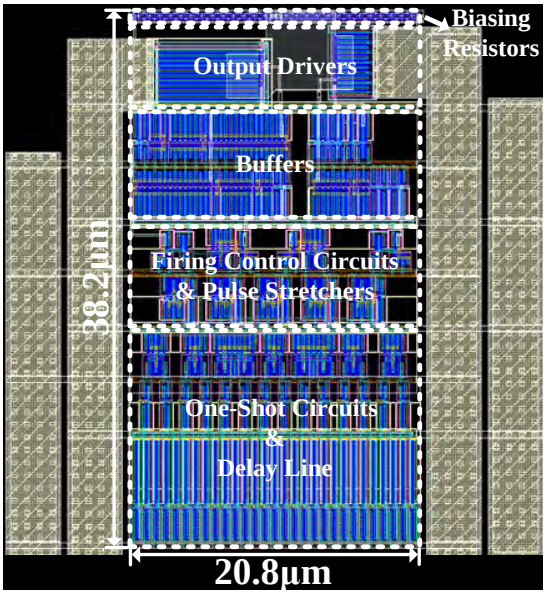

Fig. 4. PG layout.

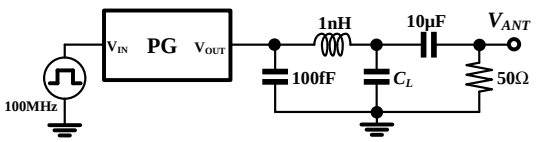

Fig. 5. PG testbench.

VI. Conclusion

A new pulse-shaping approach and a novel IR-UWB PG for a TSMC 90 nm CMOS process suitable for RFID tags have been presented. A power-efficient pulse generation is achieved by output driver re-use and simple combinatorial gates. Post-layout simulations show the worst-case power consumption

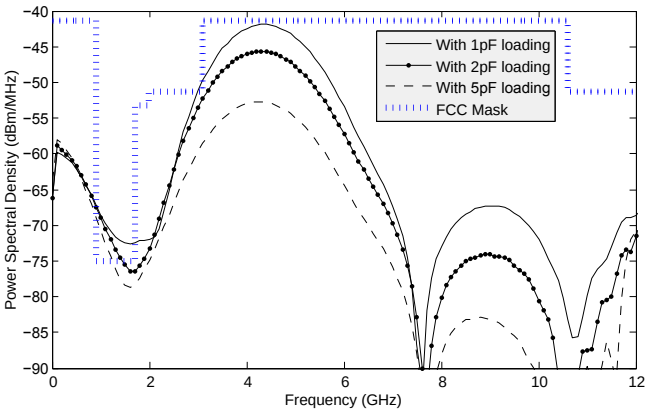

Fig. 6. Frequency spectra of the PG output with different C_L.

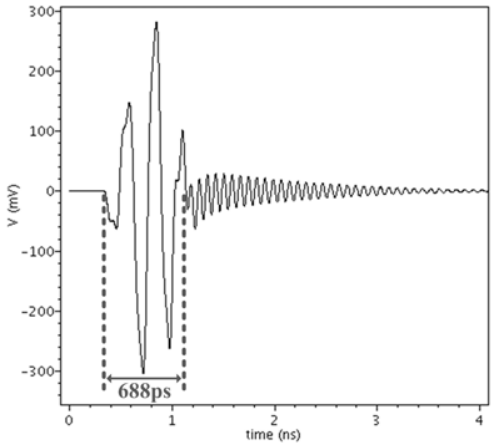

Fig. 7. Transient simulation result

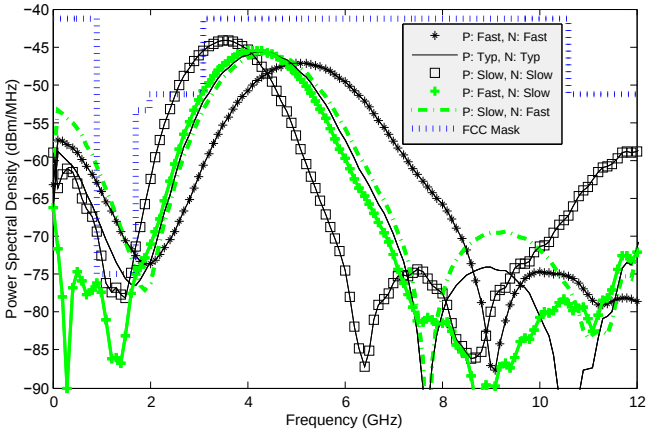

Fig. 8. Frequency spectra of the PG output at different design corners.

from a 1.2 V supply is 6.5 pJ/pulse for a 100 MHz PRF, which is suitable for ultra low-power applications. The PG contains mainly digital gates, which is very beneifical from nano-meter CMOS technology. We are expecting this IR-UWB PG to be suitable for RFID tags with on-chip power-harvesting.

TABLE I
SUMMARY OF SIMULATION RESULTS, AND COMPARSIONS TO OTHER PUBLISHED UWB-IR PGS.

Design	Tech. (CMOS)	f_{center} (GHz)	BW_{-10dB} (GHz)	τ_{OUT} (ns)	Power Diss. (pJ/Pulse)	Area (mm^2)
This work	90 nm	4.3	2.94	0.69	6.5	0.00079
[2]	130 nm	~3.1	N/A	0.75	5.6	0.02
[3]	90 nm	4.05*	0.55	3	47	0.08
[4]	180 nm	4.05	1.4	1.75	825	0.4
[5]	90 nm	3.5–10	0.5	17	40	0.066

* Two other f_{center} (i.e. 3.45 GHz and 4.65 GHz) can be selected.

ACKNOWLEDGMENT

The authors would like to thank Novelda AS for their useful suggestions on IR-UWB PG design.

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"*Our life is frittered away by detail. Simplify, simplify.*"
"*As you simplify your life, the laws of the universe will be simpler; solitude will not be solitude, poverty will not be poverty, nor weakness weakness.*"
— Henry David Thoreau

A.2 Paper-II

K. K. Lee, M. Z. Dooghabadi, H. A. Hjortland, Ø. Næss and T. S. Lande, "A 5.2 pJ/pulse impulse radio pulse generator in 90 nm CMOS," in *Proc. IEEE International Symposium on Circuits and Systems*, May 2011, pp. 1299–1302.

A 5.2 pJ/Pulse Impulse Radio Pulse Generator in 90 nm CMOS

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***Abstract*—A low-power impulse radio (IR) ultra wideband (UWB) pulse generator (PG) is presented. It uses digital gate-delay for timing achieving good power efficiency and acceptable spectral filling. The circuit is scalable in both bandwidth and center frequency. Both energy consumption and chip area are reduced compared to most conventional higher order Gaussian PGs. The PG is realized in a TSMC 90 nm CMOS process. Measurements show the energy consumption from a 1.2 V to be 5.2 pJ/pulse for a 200 MHz pulse repetition frequency (PRF). The core area is 0.0015 mm^2 (38 µm $\times$ 40 µm). Lastly, a dynamic pre-charge (DPC) scheme is proposed to eliminate the stand-by current and make the PG favorable for low-data-rate applications.**

***Index Terms*—IR, UWB, RFID, CMOS, pulse generator**

I. Introduction

Since the Federal Communication Commission (FCC) released a large spectral mask (i.e. 3.1–10.6 GHz) for unlicensed use [1], UWB technology has been an attractive field of research. The huge spectral mask not only gives the benefit of higher date rate, but also reduced power consumption of transmitting circuits by using IR technology. One potential application is RFID tags. Conventional passive RFID tags utilitize load or backscatter modulations which limits the number of channels. By using power-efficient IR-UWB technology, it is possible to apply different multiple access schemes (for example CDMA) on no-battery, energy-harvesting RFID tags. One of the most challenging tasks is to design low-power IR-UWB PG which is usually the most power-consuming component in the UWB transmitters.

A novel pulse-shape generation approach was proposed in [2], but no real prototype and measurement results were presented. In this paper, a low-power IR-UWB PG based on [2] was realized in a TSMC 90 nm CMOS process. It uses digital gate-delay for timing, achieving good power efficiency and acceptable spectral filling. The circuit is scalable in both bandwidth and center frequency. Both energy consumption and chip area are reduced compared to most conventional higher order Gaussian PGs. Measurements show the energy consumption from a 1.2 V supply to be 5.2 pJ/pulse for a 200 MHz PRF. The core area is 0.0015 mm^2 (38 µm $\times$ 40 µm). The PG performs very well, especially in terms of energy consumption and chip area, and is competitive to other recently published UWB PGs [3]–[6]. One drawback is that the output DC voltage is biased by a resistive divider. A DPC scheme is proposed to eliminate the stand-by current due to the resistive divider and make the PG favorable for low-data-rate applications.

II. Pulse-Shape Generation

Higher order Gaussian pulse-shapes are widely used in IR-UWB PGs to minimize the sideband interference, however, it is hard to generate higher order Gaussian pulses in standard CMOS processes with simple circuit solutions. A piecewise Gaussian approximation (PGA) approach was proposed in [7] and a very low-power (5.6 pJ/pulse) IR-UWB PG using a

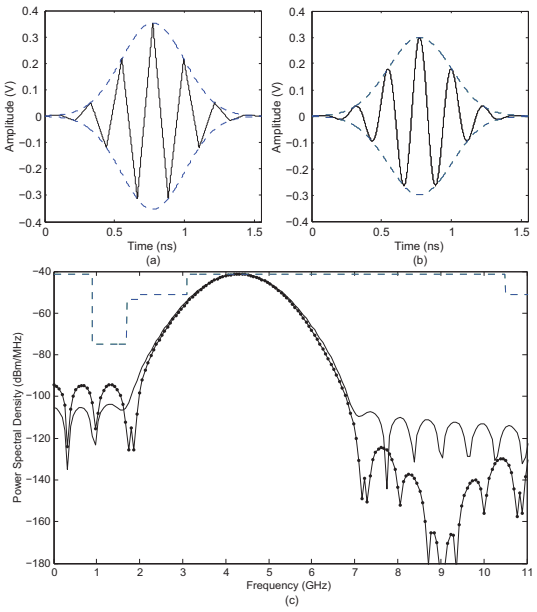

Fig. 1. (a & b) Pulse-shape generation approach. (c) Dotted: power spectrum of (a); Solid: power spectrum of (b); Dashed: FCC mask.

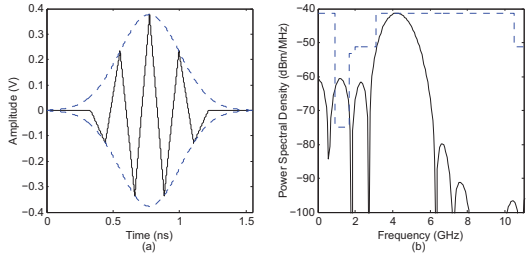

Fig. 2. (a) Adopted pulse-shape. (b) Solid: Its power spectrum; Dashed: FCC mask.

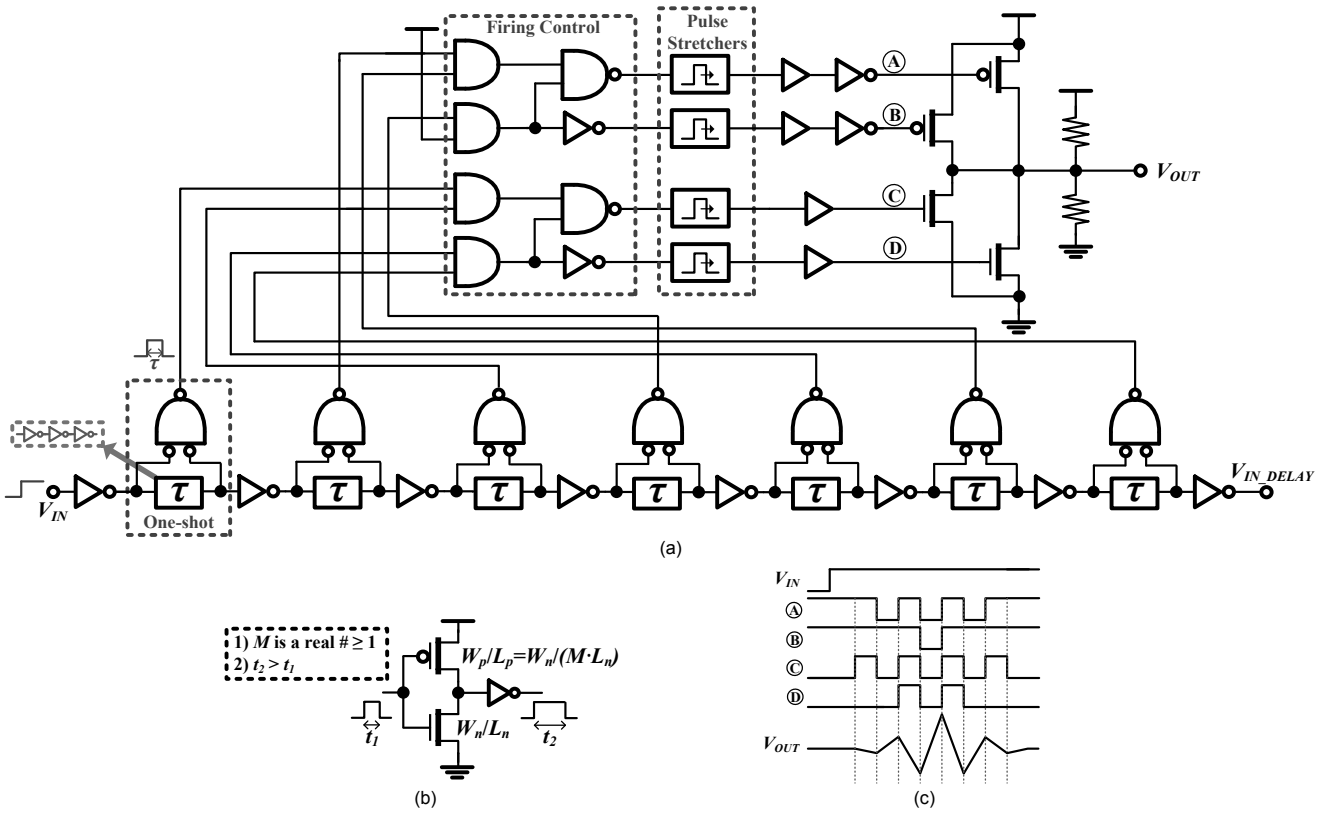

Fig. 3. (a) Designed PG. (b) Pulse stretcher. (c) Timing diagram.

similar approach was reported in [3]. The weakness is the circuit complexity, the number of generator stages and output drivers are proportional to the order of the Gaussian function. Only one output driver is used during each phase, the unused output drivers add output capacitance and, hence, increase the power consumption. Also, in order to adopt international spectral regulations (band group 6, i.e. 7.7–8.7 GHz, is the only band available worldwide [8]), a high-order Gaussian derivative (15-th) is required, but not feasible due to the increased parasitic capacitance.

Instead of generating higher order Gaussian waveforms, we use several simple pulses to construct a first order Gaussian envelope. The bandwidth (BW_{-10dB}) is then determined by the envelope width and the center frequency (f_{center}) is determined by the frequency of the generated pulses. The somehow crude generated pulses do not add significant sideband interference as long as the pulse frequency is significantly higher than the envelope frequency. The idea is depicted in Fig. 1. The amplitudes of 4.3 GHz triangular and sine waveforms are shaped to make a Gaussian envelope with α = 0.8 ns. The power spectra are shown in Fig. 1c.

Loose-triangular pulses are selected in this paper because they can be generated easily in CMOS processes by charging and discharging a parasitic capacitor. It is difficult to model loose triangular waveforms in mathematical simulators, however, its power spectrum should be somehow in between those shown in Fig. 1c. f_{center} may be limited to be 4–5 GHz in this paper because of the technology limitations. We are expecting it can be pushed to higher frequencies, hence better spectral utilization can be achieved with faster CMOS technology. The main advantage of this approach is its simplicity and technology scalability combined with power efficiency.

III. Circuit Implementation

Because the gate count is proportional to the number of triangular pulses generated, the weak pulses at the beginning and at the end of the pulse-sequence are omitted in order to simplify the circuit and minimize the power consumption. The resulting waveform and power spectrum is shown in Fig. 2. The f_{center} is 4.2 GHz with a BW_{-10dB} of 2.3 GHz. Some low-frequency sidebands are observed. However, simulations show that the mismatch between the charging and discharging time is the main reason for low-frequency sidebands and omission of the weak pulses does not have a significant impact on the sidebands. The low-frequency sidebands may be reduced by adding high-pass filters, or even just exploring the antenna band-pass property.

The schematic of the PG is depicted in Fig. 3a. The structure is similar to the PGA-PG in [3], but the idea is different. The designed PG contains only simple digital gates and does not have any Gaussian pulse generators. The one-shot circuit is triggered by a falling edge and creates a fixed-width pulse τ.

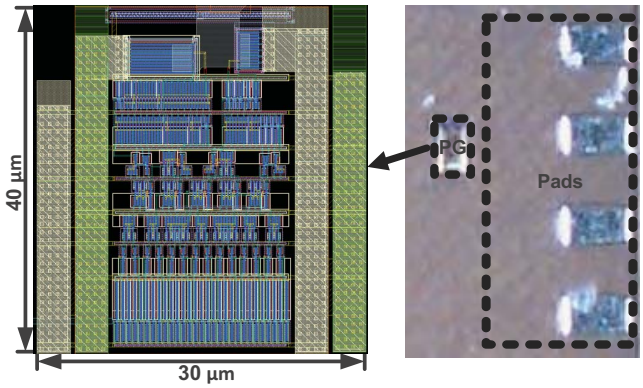

Fig. 4. (Left) Circuit Layout. (Right) Die photo.

Pulse stretchers [9] (schematic shown in Fig. 3b) are added to adjust the width of the pulses in order to minimize the sideband energy. High threshold transistors are used for the delay line to minimize the leakage current.

As mentioned, in PGA-PGs, only one output driver is on in a single phase, the unused output drivers add undesired output capacitance and degrade the circuit performance. In the designed PG, only loose-triangular waveforms are generated, this makes it possible to share the output drivers like the timing diagram shown in Fig. 3c. One or more output drivers with different strength are combined for desired charging and discharging strength, which is a very important feature for generating multi-cycles IR-UWB pulses. The firing control logic is required for correct firing sequence. The last pull-up is due to the output resistive divider. We can see that the PG contains only digital gates for timing, exploring inherent gate-delays.

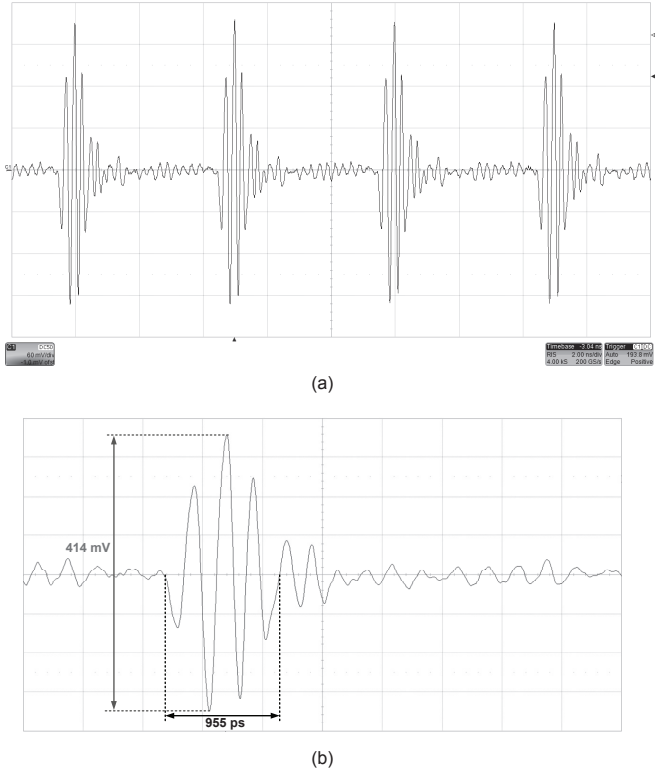

Fig. 5. (a) Output waveform for a 200 MHz PRF and (b) its zoom-in.

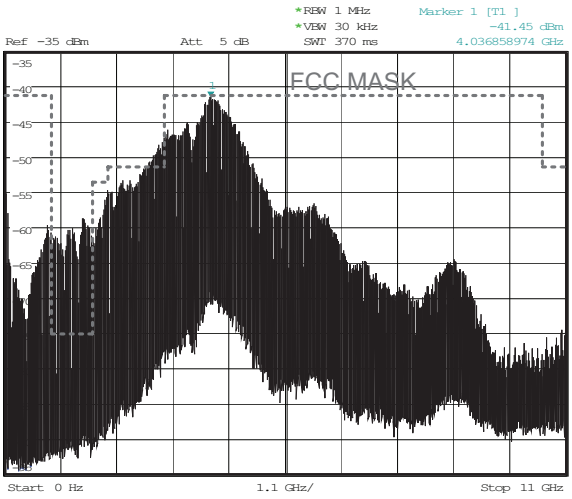

Fig. 6. Measured power spectrum.

IV. Experimental Results

The PG is realized in a TSMC 90 nm CMOS process. A die photo is shown in Fig. 4. Since the PG contains mainly digital logics, we achieve a small silicon area of 0.0015 mm^2. The die is packaged in a 48-leads QFN package.

Fig. 5 shows the output waveforms for a 200 MHz PRF. The pulse width (τ_{out}) is 955 ps and the peak-to-peak voltage is 414 mV, the ringing is due to the bondwire inductance.

TABLE I
Measured Energy Consumption at Different PRF.

PRF (MHz)	Energy Cons. (pJ/Pulse)
1	67.5
5	17.3
10	11.2
20	8.1
40	6.5
100	5.6
150	5.4
200	5.2

TABLE II
Simulated Energy Consumption with/without DPC Scheme at Different PRF.

PRF	Energy Cons. (pJ/Pulse)	
(MHz)	w/ DPC	w/o DPC
0.5	5.4	129.1
1	5.3	66.9
5	5.2	17.2
10	5.2	11.0
20	5.2	7.9
50	5.1	6.0

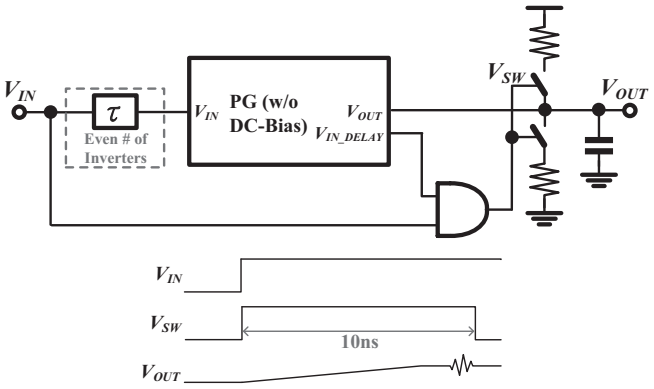

Fig. 7. DPC scheme.

Its power spectrum is depicted in Fig. 6. f_{center} is 4 GHz approximately and BW_{-10dB} is around 1.9 GHz (i.e. 2.89–4.81 GHz), which are very close to our expected values. With faster CMOS processes, we can push f_{center} to higher frequencies and achieve better spectral utilization.

Table I shows the measured energy consumption at different PRF. When the PRF is 200 MHz, the PG shows the lowest energy consumption of 5.2 pJ/pulse for a 1.2 V supply. However, the energy consumption increases when the PRF decreases. It is because the resistive divider is used to bias the output DC voltage and drives static current. This makes it difficult to apply the designed PG on low-data-rate applications.

V. Dynamic Pre-Charge

To eliminate the stand-by current consumption, a DPC scheme is proposed. The proposed circuit is shown in Fig. 7, the biasing resistors are connected to the output a short time before the pulse is transmitted and disconnected immediately after the radiation. The resistors and, hence, the time constant of pre-charging should be set reasonably large, otherwise the antenna may radiate unwanted EM energy during pre-charging.

Table II shows the pre-layout simulation results on the PG energy consumption with/without DPC. We can see that the stand-by energy consumption is greatly reduced with the DPC scheme and this makes the PG suitable for low-data-rate applications. The only stand-by component is now the leakage current. Thanks to the new efficient pulse-shape generation approach, we use only a very small silicon area and the leakage current is insignificant[1] compared to the total energy consumption.

VI. Conclusion

A low-power IR-UWB PG has been presented. It has been realized in a TSMC 90 nm CMOS process. It makes use of a new pulse-shape generation algorithm which is suitable for CMOS implementation. Measurements confirm the energy consumption from a 1.2 V supply to be 5.2 pJ/pulse for a 200 MHz PRF. The core area is 0.0015 mm^2 (38 µm × 40 µm). Also, a DPC scheme has been proposed to eliminate the stand-by current and makes the PG suitable for low-data-rate applications. A summary of the measurement results and comparison to some recently published IR-UWB PGs [3]–[6] are given in Table III. We can see that the PG performs very well, especially in term of energy consumption and chip area, and is competitive to other state-of-the-art IR-UWB PGs.

TABLE III
Summary of Measurement Results, and Comparsion to Other Published IR-UWB PGs.

Design	Tech. (CMOS)	f_{center} (GHz)	BW_{-10dB} (GHz)	τ_{out} (ns)	Energy Cons. (pJ/Pulse)	Area (mm^2)
This work	90 nm	4	1.92	0.96	5.2	0.0015
[3]	130 nm	~3.1	N/A	0.75	5.6	0.02
[4]	90 nm	4.05*	0.55	3	47	0.08
[5]	130 nm	N/A	6.8	0.46	38.4	0.54
[6]	180 nm	~8	3.9	0.6	14	0.11

* Two other f_{center} (i.e. 3.45 GHz and 4.65 GHz) can be selected.

Acknowledgment

The authors would like to thank Novelda AS for their useful suggestions on IR-UWB PG design.

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[1]The leakage current is usually proportional to the transistor width. For digital circuits, minimum length is commonly used, which means the total leakage current is proportional to the silicon area.

"*The smallest seed of faith is better than the largest fruit of happiness.*"

— Henry David Thoreau

A.3 Paper-III

K. K. Lee, H. A. Hjortland and T. S. Lande, "IR-UWB technology on next generation RFID systems," in *Proc. NORCHIP*, Nov 2011, DOI: 10.1109/NORCHP.2011.6126697.

IR-UWB Technology on Next Generation RFID Systems

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***Abstract*—Radio-frequency identification (RFID) systems are widely used in our daily life. Although several proposed solutions are in production, limitations are still significant. In this paper, the current RFID technology is reviewed and major shortcomings are discussed. Our expected features on next generation RFID systems are described. Finally, we propose an impulse-radio (IR) ultra-wideband (UWB) RFID system and present how to improve the performance by using IR-UWB technology.**

***Index Terms*—IR, UWB, RFID, CMOS, Continuous-Time Binary Value (CTBV)**

I. Introduction

RFID has been recognized as one of the most important technologies in the 21st century and permeates our daily life everywhere. One of the most challenging tasks is design RFID tags[1] with satisfying functions and, at the same time, low-cost. RFID tags nowadays can be divided into three main catalogs [1]:

a) Passive RFID tags: are the most commonly used type nowadays because there is no battery inside the tag which makes them low cost and small. The signal and energy are sent from the reader by EM/inductive coupling with a distance up to several meters. Load modulation is usually used for communication and channel separation is done by TDMA. One problem is that the tags are using the same frequency for power-harvesting and communication. When a tag is too close to the other tags, they will interfere with each other and the performance will be degraded [2].

b) Active RFID tags: are essentially radio transceivers and contain a battery. The battery gives the possibility of building up more reliable communication, however it increases the cost and product size. Also, they use narrowband technology to communicate with the reader, which is influenced by multi-path fading.

c) Semi-passive RFID tags: are a mix of *a)* and *b)*. They use load modulation for communication and contain a battery for supplying energy to the digital control circuits. This provides a stable power source and eliminates the needs of power-harvesting, hence the communication distance is increased. Again, the battery increases the cost and product size.

Moreover, all these three types of RFID tags are using narrowband technology which is difficult to provide precise localization. We can see that the limitations on the current RFID tags are still significant. For the next generation RFID tags, we are expecting they can achieve the following features:

- Low cost — small die size, no battery.
- Accurate localization without substantial cost.
- High flexibility — small size, reasonable number of channels (tags) and communication distance.
- Insensitive to the surrounding environment.

In this paper, we propose an IR-UWB RFID system with a uni-direction communication scheme and present how this system achieves the features mentioned above in section II. In section III, the required circuits are discussed. Section IV concludes the paper.

II. Proposed IR-UWB RFID System

Since the Federal Communication Commission (FCC) released a large spectral mask (i.e. 3.1–10.6 GHz) for unlicensed uses [3], UWB technology has been an attractive field of research. The huge spectral mask not only gives the benefit of higher date rate, but also reduced power consumption of transmitting circuits by using IR technology.

The short pulse width (high bandwidth) and the impulse nature of IR-UWB signals enable the possibility of implementing accurate localization [4], several UWB localization approaches were presented in [5]. Moreover, IR-UWB systems are resistant to severe multi-path fading and jamming [6] and this increases the quality of communication[2]. Some applications requires high security, the noise-like nature of UWB signals makes it difficult for unintended users to detect. Because of these advantages, we expect the performance of RFID systems can be improved by using IR-UWB technology.

A simplified block diagram of the proposed RFID systems is shown in Fig. 1. To eliminate the interference problems between the tags and minimize the tags circuit complexity, the proposed IR-UWB RFID system utilizes uni-directional communication — the reader transmits UHF signals for energy-harvesting purposes only (without any data), the tags start sending out their unique ID when they harvest enough energy. The channel separation is done by using CDMA and an "inherent ALOHA" property of the system.

[1]Some RFID tags in the market embed sensor and memory circuits to increase user satisfactory, which is a bit overlapping with the wireless sensor network area. In this paper, the RFID tags mean those are used for purely identification purposes.

[2]This is especially important for energy-limiting circuits like RFID tags because we do not have enough energy budget to implement advanced communication protocols.

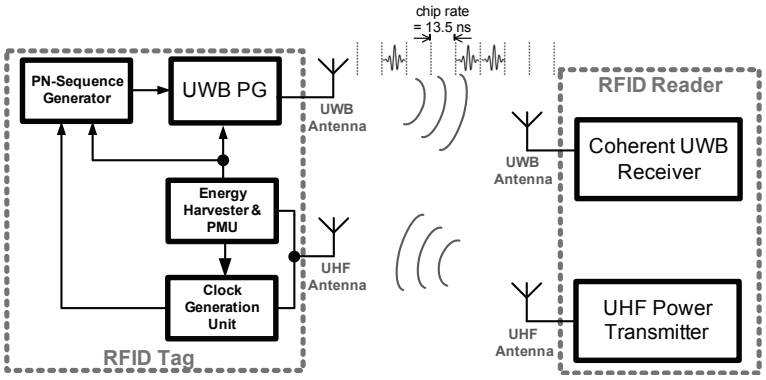

Fig. 1. The proposed IR-UWB RFID system.

A. Operations of the Propose IR-UWB RFID Systems

The operations are briefly described below and more information about the required circuits is given in the next section.

- The reader sends out UHF signal.
- The tags harvest energy and generate a clock signal using the UHF signal. A critical design parameter is the chip rate used for symbol encoding.
- Every tag is assigned with a symbol (its unique ID) which consists of n-bits pseudonoise (PN) code (a small n of 8 is used in this example for simplicity). Details of code design and channel separation are presented in the next sub-section. The chip rate is set to around 13.5 ns (depends on the UHF signal frequency approximately 860–960 MHz) to avoid inter-chip-interference[3]. When the tag harvests enough energy, the tag sends out its symbol through the on-off key IR-UWB pulse generator (PG) and the UWB antenna.
- The coherent UWB RAKE receiver inside the reader detects and checks the received symbol.
- Repeat the above steps a certain number of times to get higher processing gain[4].
- The localization requires several receivers and the localization accuracy is improved by the number of receivers.

B. Channel Seperation and Code Design

In the current RFID systems, TDMA is usually adopted and this requires a fully synchronous communication between the tags and the reader. Nevertheless, for UWB systems, the signals are usually transmitted repeatedly (can be a few ten thousand times) to get enough processing gain. If there are a large number of tags, it will be difficult to apply TDMA on such busy systems.

Instead, an uni-directional asynchronous CDMA (A-CDMA) communication scheme is utilized in our design[5]. The tags keep transmitting whenever they harvest enough energy and are identified using A-CDMA. This eliminates the synchronization between the tags and the reader and we can establish a reliable communication if the tags and the reader have the consensus on the chip size. Every tag is assigned with a symbol, which is constructed using 64-b large set Kasami codes. This gives a max of 520 (i.e. $2^{(\log_2 n/2)} \cdot (2^{\log_2 n} + 1)$) channels with a max cross-correlation function (CCF) of 16-b [9].

When the reader receives the signals, it compares the received symbol and stored symbols of all tags. If the matching level is higher than a pre-set threshold value (let's say $2\times$ of CCF, i.e. 32-b), we can assume the tag is detected.

Moreover, the proposed system has an inherent ALOHA property — every tag needs different time to harvest energy due to process variation, component mismatch and distance to the reader etc., the transmission slot of the tags tends to be random, which acts like an ALOHA system. As long as the transmission duty cycle is small[6], the probability of collision is greatly reduced. Also, since all the tags keep transmitting for a certain number of times, even a few transmissions have severe interference, this can be compensated by digital signal processing.

For some applications like logistics, more channels are preferred. This can be done by:

- *Increasing the length of the symbol*. Nevertheless, this increases circuit complexity and energy consumption.
- *Changing the code family*. For example, if very large Kasami code is used, the max number of channels becomes $2^{(\log_2 n/2)} \cdot (2^{\log_2 n} + 1)^2$ [9]. However, the CCF

[3]We adopt the IEEE UWB LOS channel model in [7] with a rms delay spread of 5.28 ns.

[4]For UWB systems, the emission energy is very small (for example, FCC UWB part 15 regulation limits the emission energy to be –41.3 dBm/MHz). The data are usually sent repeatedly to get higher processing gain (i.e. increasing the signal-to-noise ratio by averaging out the noise), hence the communication distance is increased. Some UWB radars [8] using this approach was reported to achieve a max detection distance of 60 m.

[5]One of the final goals is to design RFID tags harvesting energy from the environment, not from the reader (for example, light, temperature, human movement etc. Unfortunately, to the best of the authors' knowledge, such kind of energy harvesting approaches with stable performance are still not available). Synchronization between the tags and the readers becomes difficult. This is another reason why the uni-directional A-CDMA is adopted.

[6]The transmission duty cycle is defined as the ratio of the transmission time to the energy-harvesting time. In this case, the transmission time is $64 \cdot 13.5$ ns = 864 ns and the energy-harvesting time is usually with the order of 10 ms.

Fig. 2. The clock generation unit.

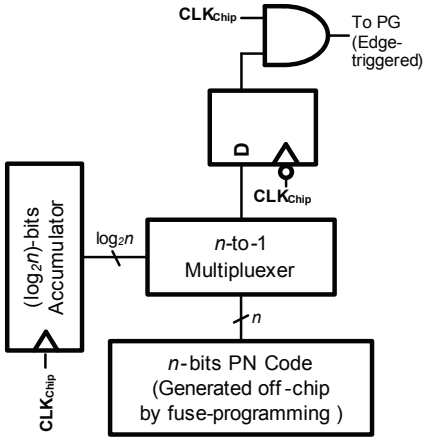

Fig. 3. The PN sequence generator.

also increases and we need to decrease the transmission duty cycle to maintain the same collision rate.

III. Circuit Design

A. Circuits Inside the Tags

The tags consist of a clock generation unit, an energy harvester, a power management unit (PMU), an IR-UWB PG and some digital circuits, see Fig. 1.

1) Clock generation unit: The clock generation unit contains an injection-locking frequency divider (ILD) and digital dividual-by-2 frequency dividers, the block diagram is shown in Fig. 2. Several clock generation approaches for conventional RFID tags are discussed in [10]. The ILD approach is chosen in this paper because it is reported to be one of the most precise without trimming (remember that our system requires an accurate chip rate). Although it is a bit power-consuming (the lowest of 7 μW was reported in [11]), the most energy-demanding component in our system is still the IR-UWB PG.

2) IR-UWB PG: Delay-line based IR-UWB PGs are widely used since they do not need precise high-frequency carrier generators and, thus, can be very low-power. We proposed a new PG structure in [12] and a PG using this structure shows an energy consumption of 5.2 pJ/pulse [13]. One concern is the delay line speed (hence the spectrum center frequency of the PG output) varies under PVT variations, this can be remedied by using continuous-time binary value (CTBV)[7] receivers which will be discussed later in this section.

3) Digital circuits: The digital circuits include mainly digital control circuits (which are not discussed here) and a PN sequence generator. Its block diagram is shown in Fig. 3. The PN code of individual tag is assigned by fuse-programming off-chip and shifted-out every chip-cycle.

[7]CTBV is a signal-processing domain proposed in [14].

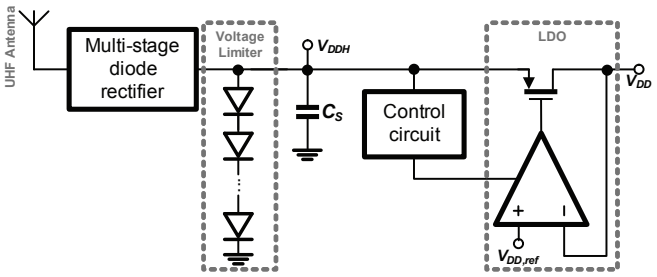

Fig. 4. The power management unite.

4) Energy harvester and PMU: The simplified block diagram is shown in Fig. 4. The structure is similar to the ones used in conventional RFID systems and contains a multi-stage diode rectifier, a low-dropout voltage regulator (LDO) and a voltage limiter [15]. However, because of the power-demanding UWB PG, we need to modify the structure so as to harvest more energy. During energy-harvesting, a control circuit is required to turn off the LDO until V_{DDH} is higher than a certain level so that the loading current is minimized. More charge, hence more energy, will accumulate in the storing capacitor C_S as long as the harvesting energy is higher than the total energy consumption of the control circuit and leakage. Similar idea was used in [16] and it shows a possibility of sending >1k IR-UWB pulses after an energy-harvesting time of a few 10 ms. The voltage limiter limits V_{DDH} to prevent oxide breakdown.

5) Power budget breakdown: The worst-case total energy consumption of the PG is 5.2 pJ/b · 64-b = 333 pJ and assume the other circuits and leakage consumes 20% energy of the PG, the total energy consumption of the whole tag (E_{Tag}) is then 400 pJ during a single transmission phase. Assume the dropout voltage is 200 mV, V_{DD} is 1.2 V and the LDO is turned on when $V_{DDH} > 2.5$ V then off when V_{DDH} drops to 1.4 V. If the V_{DDH} decreases linearly with time, the loss due to the LDO is:

$$E_{Loss,LDO} = \frac{E_{Tag}}{V_{DD}} \cdot \left(\overline{V_{DDH}} - V_{DD}\right) = 250 \text{ pJ} \quad (1)$$

As a result, the total energy consumption for the transmissions is around 650 pJ. Then the size of the C_S can be found as:

$$E_{Tag} + E_{Loss,LDO} = \frac{1}{2} C_S \left(\overline{V_{DDH}} - V_{DD}\right)^2 \quad C_S \approx 2.3 \text{ nF} \quad (2)$$

which would be possibly integrated on-chip.

B. Circuits Inside the Readers

The reader mainly consists of a high-output-power UHF signal generator (which is not discussed here) and a coherent UWB receiver. The coherent UWB receivers is adopted here because it gives better localization ability, for example an coherent receiver was used in [17] and the achieved resolution was shown to be 4.3 mm.

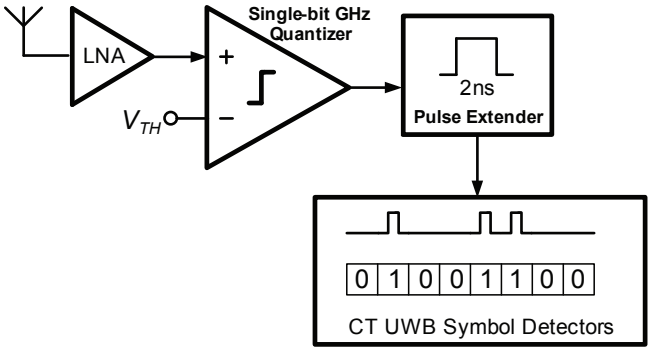

Fig. 5. An example coherent UWB receiver.

An coherent CTBV UWB RAKE receiver proposed in [18] is used as an example here, its simplified block diagram is shown in Fig. 5. First the LNA amplifies the received signal, the signal is then quantized by the single-bit quantizer and the resultant CTBV signal is time-extended (let's say 2 ns). Finally the CTBV symbol detector, which contains no clock, compares the received symbol with the stored symbol.

The clock-less structure eliminates the clocking circuits, this reduces the circuit complexity and makes it power-efficient. As mentioned above, the delay-line IR-UWB PGs are usually sensitive to PVT variations, the CTBV receiver uses time-domain processing and is insensitive to the frequency variation as long as the PG signal is within the passband of the UWB antenna and the LNA.

IV. Conclusion

The ubiquity of RFID systems in everyday life is increasing rapidly, however, limitations are still significant. We have listed some expected features for next generation RFID systems and presented how to improve the RFID system using IR-UWB technology. A IR-UWB RFID system has been proposed and the required circuits have been discussed to prove the system workable. To summarize, compared to conventional RFID counterparts, the proposed system has the advantages of accurate localization, insensitivity to the surrounding environment and high security.

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"*It is only when we forget all our learning that we begin to know.*"
"*It is never too late to give up our prejudices.*"

— Henry David Thoreau

A.4 Paper-IV

K. K. Lee and T. S. Lande, "Analysis and design of sub-μW bandgap references in nano-meter CMOS", in *Proc. IEEE International Midwest Symposium on Circuits and Systems*, Aug 2013, pp. 93–96.

Analysis and Design of Sub-μW Bandgap References in Nano-Meter CMOS

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***Abstract*—Analysis and design of nano-watt (nW) bandgap references (BGR) in nano-meter (nm) CMOS are presented. Three different BGR topologies are studied and design trade-offs are discussed. Based on the analysis results, a BGR is fabricated in a TSMC 90 nm CMOS process. A special feature is that it can generate proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) current individually which enables more possibility of system co-design. Measurements show temperature coefficient and line sensitivity without trimming are 47.1 ppm/°C and 0.8 %/V respectively. The power consumption of the BGR core with a 1.2 V supply is 315 nW at room temperature. The core area is 0.026 mm^2.**

***Index Terms*—Bandgap references, nano-meter CMOS, wireless sensor networks, low-power**

I. Introduction

Wireless sensor networks (WSN) have been an active research topic in recent years. For such applications, the system power consumption has to be minimized in order to increase the battery life, or even enables wireless powering, thus the maintenance cost and product size can be reduced. Also, the system has to be insensitive to the temperature and voltage variations because the operating environment may not be well-controlled.

One important component is voltage (or current) reference generator for biasing other circuits. BGRs have been used for decades because of their reliability. However most BGRs contain resistors and large amount of resistance is needed to reduce the power consumption to the order of sub-μW, this may increase the chip area substansiously. As a result, some research [1] [2] has been conducted on CMOS-only voltage references, the trade-off is the relatively large error due to process variation [1]. Thanks to the continuing aggressive scaling of CMOS technology, highly-compact resistors can be achieved in the state-of-the-art CMOS processes (for example a 7.9 MΩ resistance with a area of only 4340 μm^2 is achieved using a 90 nm CMOS process in this paper). The resistor area is now not dominating, and becomes comparable to the other required components (i.e. BJT and MOS transistors). This makes BGR to be a potential candidate for such applications.

In this paper, three different kinds of CMOS BGRs are studied and compared in different aspects including power consumption, area, functionality and flexibility etc. A nW CMOS BGR for WSN applications is realized in a TSMC 90 nm CMOS process and its performance is competitive compared to other state-of-the-art CMOS references.

II. Different Kinds of BGR

A. BGR Structure #1

Fig. 1 shows one of the very widely-used BGRs and it will be referred to as BGR-1. For vertical BJTs in normal CMOS processes, the emitter current is given by [3]

$$I_E = I_S e^{\frac{V_{BE}}{n \cdot V_T}} \tag{1}$$

where I_S is the saturation current, V_T is the thermal voltage and n is the emission coefficient. We assume the base current is small and the voltage drop across the base resistance is ignorable. Because the emitter area of Q2 is N times that of Q1 (i.e. $I_{S2} = N \cdot I_{S1}$), we can write

$$I_O = \frac{n \cdot V_T}{R_1} \ln\left(\frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}}\right) \approx n \cdot V_T \frac{\ln(N)}{R_1} \tag{2}$$

Hence,

$$V_O = V_{EB3} + n \cdot \ln(N) \frac{R_2}{R_1} \cdot V_T \tag{3}$$

By sizing N and the ratio between R_1 and R_2, such that

$$M = n \cdot \ln(N) \frac{R_2}{R_1} = \left| \frac{\overbrace{\partial V_{BE}/\partial T}^{\approx -1.6\ \text{mV/°C}}}{\underbrace{\partial V_T/\partial T}_{\approx 85\ \mu\text{V/°C}}} \right| \tag{4}$$

V_O will be, to the first order, temperature independent. It is fixed to be around 1.2 V due to the silicon energy bandgap [4]. The total amount of resistance is a good indicator to compare the area of different structures. Assume all the PMOS current mirrors have the same size,

$$R_{Total} = \frac{nV_T \cdot \ln(N)}{I_O} \left(1 + \frac{M}{n \cdot \ln(N)}\right) = R_a(1 + K) \tag{5}$$

BGR-1 is simple and small in area compared to other BGR topologies, which will be shown later. The major problem of BGR-1 is the minimum supply voltage (V_{DD}), it has to be large than 1.2 V + V_{DS3}. This limits its usability in state-of-the-art nm CMOS processes which are targeted to operate at low V_{DD} in order to minimize the power consumption. Also, multiple reference voltage may be needed for large systems. For BGR-1, voltage buffer is needed in order to do this, this increases the power consumption and complexity.

B. BGR Structure #2

In order to lower the minimum V_{DD}, Banba *et al.* [5] proposed the structure (will be referred to as BGR-2) shown in Fig. 2. The amplifier introduces a low-frequency pole, hence C_C may be needed for stabilization purposes [3]. The amplifier inputs are forced to have the same voltage and if we ignore the amplifier offset, similar to (1), I_{PTAT} can be found as

$$I_{PTAT} \approx n \cdot V_T \frac{\ln(N)}{R_1} \tag{6}$$

Notices $R_2 = R_3$ and R_2 generates an I_{CTAT} as

$$I_{CTAT} = \frac{V_{EB1}}{R_2} \tag{7}$$

Thus,

$$V_O = n \cdot \ln(N) \frac{R_4}{R_1} V_T + \frac{R_4}{R_2} V_{EB1} \tag{8}$$

And the total amount of resistance is given as:

$$R_{Total} = R_1(1+2K) + \frac{V_O}{I_O} = L \cdot R_a(1+2K) + \frac{V_O}{I_O} \tag{9}$$

where

$$L = \frac{I_O}{I_{PTAT}} > 1 \tag{10}$$

Notice that V_O can be varied by changing the ratio of R_4/R_1 and R_4/R_2 and the minimum V_{DD} is now given as $V_{EB1} + V_{DS1}$ (around 800–900 mV). In addition, BGR-2 also provides the possibility of generating temperature independent current reference and multiple reference voltage (by replacing R_4 with multiple resistors with desired values in series) easily.

The trade-offs are the area and power consumption due the amplifier and C_C, the total amount of resistance is also larger than other BGR topologies for the same power consumption. Moreover, the amplifier offset will contribute to V_O and introduces another PTAT parameter, this increases the design difficulty.

C. BGR Structure #3

In nm CMOS processes, deep N-well layer is normally available, which enables the usage of NPN BJTs with moderate quality. Yin *et al.* [6] proposed a structure using NPN BJTs (will be referred to as BGR-3), the schematic is shown in Fig. 3. Assume the base current is small and ignorable, we can obtain

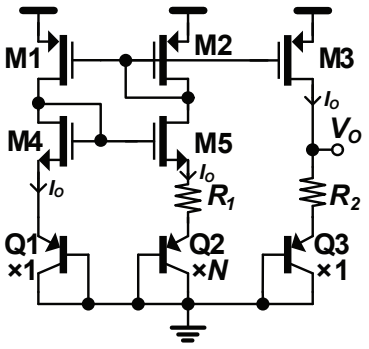

Fig. 1. A widely-used BGR (BGR-1).

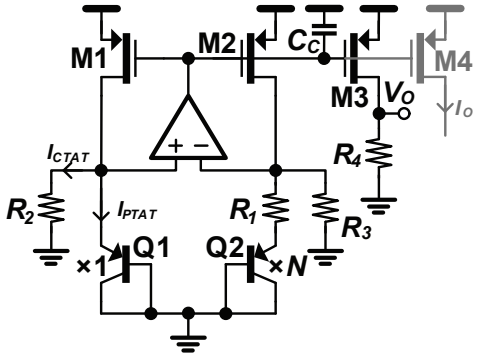

Fig. 2. BGR proposed by Banba *et al.* (BGR-2).

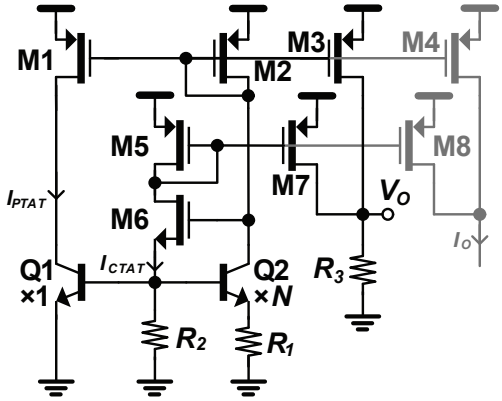

Fig. 3. BGR proposed by Yin *et al.* (BGR-3).

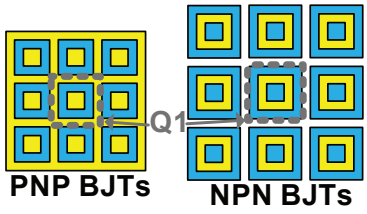

Fig. 4. Layout of PNP and NPN BJTs (only diffusion shown).

$$I_{PTAT} \approx n \cdot V_T \frac{\ln(N)}{R_1} \tag{11}$$

and

$$I_{CTAT} \approx \frac{V_{BE1}}{R_2} \tag{12}$$

As a result,

$$V_O = n \cdot \ln(N) \frac{R_3}{R_1} V_T + \frac{R_3}{R_2} V_{BE1} \tag{13}$$

And the total amount of resistance can be found as:

$$R_{Total} = R_1(1+K) + \frac{V_O}{I_O} = L \cdot R_a(1+K) + \frac{V_O}{I_O} \tag{14}$$

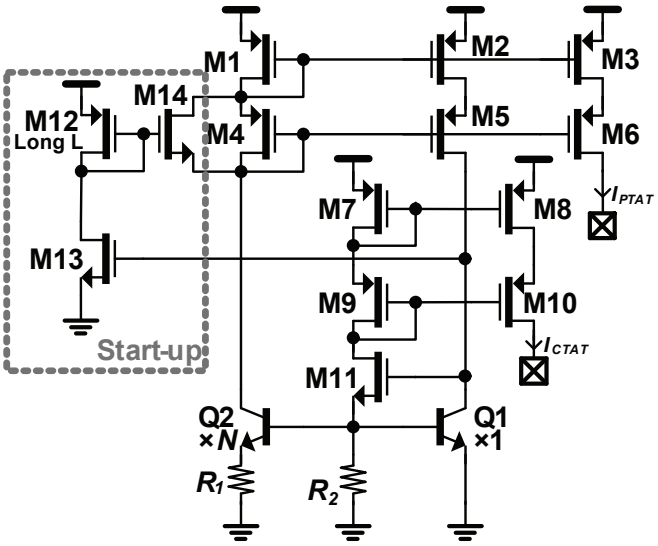

Fig. 5. Designed BGR.

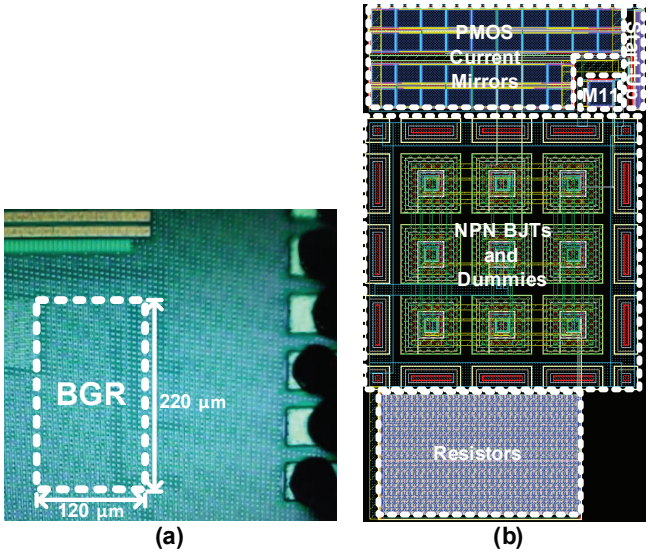

Fig. 6. a) Chip photo and b) BGR layout.

TABLE I
A COMPARISON BETWEEN THE THREE DIFFERENT BGRS.

	BGR-1	BGR-2	BGR-3
Sub-1.2V V_{DD}	No	Yes	Yes
Multiple output references possible	No	Yes	Yes
Area	+	– –	–
Power consumption	+	–	+
Design difficulty	+ +	–	+
System co-design	–	–	+
Temperature-insensitive current reference available	No	Yes	Yes
Extra masks	No	No	Maybe

Similar to BGR-2, BGR-3 can achieve multiple current and voltage references, variable output voltage and sub-1.2V V_{DD} (minimum $V_{DD} \approx V_{BE1} + V_{DS2} + V_{GS6}$). However, it is comparatively simpler and easier to design. It also has a very interesting feature, by sizing output current mirrors (M4 and M8 in Fig. 3) individually, we can control the slope of the I_O vs. temperature curve. Such behavior provides more possibilities for system co-design, for example we can compensate the circuit temperature variation by controlling their bias current properly. Such idea was applied to design temperature compensated circuits and temperature sensors etc [6].

The major disadvantage of BGR-3 is the large area due to the NPN BJTs. Unlike the other two BGRs, the collector inputs of Q1 and Q2 are not connected together, this increases the area significantly (can up to 30 % for the same emitter size, the situation is illustrated in Fig. 4). Also, due to the thickness of the deep N-well, the minimum size of NPN BJTs and spacing between them are much larger compared to the PNP BJTs case, which potentially increases the area. Notice that the deep N-well layer may require extra masks and increase fabrication cost.

D. Comparsion Between Three Structures

Table I summarizes the pros and cons of the three different structures. BGR-1 has the smallest area and is easy to design, but worst flexibility. BGR-3 shows a good performance in most areas except potential extra masks needed. BGR-2 is a compromise between these two structures.

III. EXPERIMENTAL RESULTS

BGR-1 and -2 have been widely reported and discussed, however limited experimental results have been reported for BGR-3 [6]. A BGR-3 is designed to get more insight, it is realized in a TSMC 90 nm CMOS process. Its schematic is shown in 5. Cascode current mirrors with large transistors are used to minimize mismatch. The I_{PTAT} and I_{CTAT} are outputted and measured off-chip.

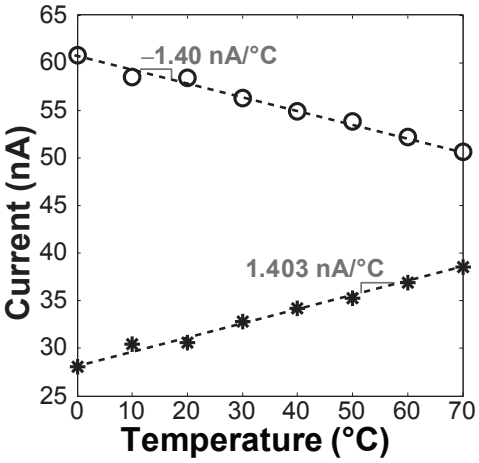

Fig. 7. I_{PTAT} (o) and I_{CTAT} (*).

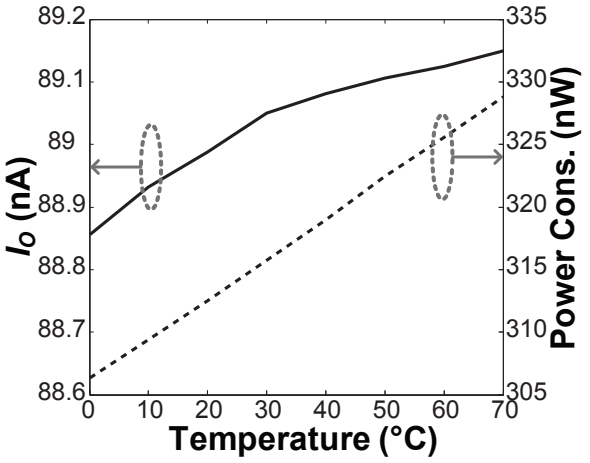

Fig. 8. Bandgap current output (solid) and power consumption (dashed).

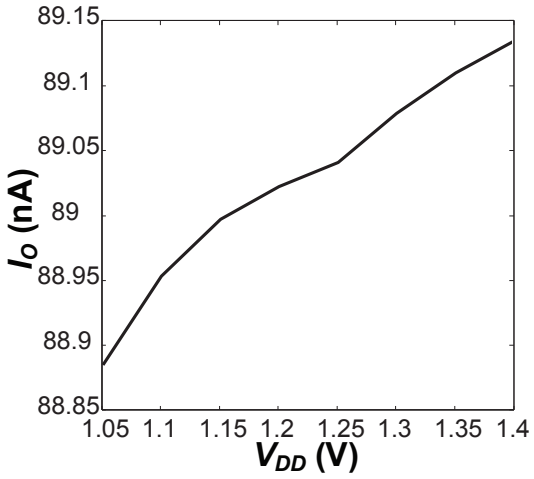

Fig. 9. Bandgap current output vs. V_{DD}.

A chip photo and the layout are shown in Fig. 6, the core area is 0.026 mm^2. The measured I_{PTAT} and I_{CTAT} are shown in Fig. 7. From 0 to 70 °C, the changes of I_{PTAT} and I_{CTAT} are 1.403 nA/°C and –1.40 nA/°C approximately. Fig. 8 shows the bandgap current output and power consumption of the BGR core including start-up circuit vs. temperature. The temperature variation without trimming is 47.1 ppm/°C. At room temperature, the power consumption with a 1.2 V V_{DD} is 315 nW and post-layout simulations show the start-up circuit consumes approximately 36 nW. The bandgap current output vs. V_{DD} at room temperature is shown in Fig. 9. The BGR starts to function properly when $V_{DD} \geq 1.05$ V and shows a line sensitivity of 0.72 nA/V (0.8 %/V). A comparison with other published CMOS references is shown in Table II.

TABLE II
A COMPARISON WITH OTHER PUBLISHED CMOS REFERENCES.

	This work	[7]	[8]	[1][a]
Technology	90 nm CMOS	0.35 μm CMOS	90 nm CMOS	0.35 μm CMOS
Min. V_{DD} (V)	1.05	2.5	0.6	0.9
Power consump. (μW)	0.315	95	450	0.036
Temp. range (°C)	0 to 70	–50 to 150	0 to 100	0 to 80
Temp. Coeff. (ppm/°C)	47.1	13.7	263	10
Line sensitivity (%/V)	0.8	0.039	3	0.27
Area (mm^2)	0.026	0.1019	N/A	0.045

[a] Non-bandgap voltage reference.

IV. CONCLUSION

Three different kinds of nm CMOS BGRs have been studied and compared. Based on the analysis results, a BGR has been realized in a TSMC 90 nm CMOS process. The designed BGR shows a competitive performance, especially in term of area and power consumption. This proves the possibility of implementing low-power, small-area BGRs in nm CMOS processes for WSN applications.

ACKNOWLEDGMENT

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"*Not only must we be good, but we must also be good for something.*"

— Henry David Thoreau

A.5 Paper-V

K. K. Lee, T. S. Lande, and P. D. Häfliger, "A sub-μW bandgap reference circuit with an inherent curvature-compensation property," *IEEE Transactions on Circuits and Systems I: Regular Papers*, to be published, DOI: 10.1109/TCSI.2014.2340553.

A Sub-μW Bandgap Reference Circuit with an Inherent Curvature-Compensation Property

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***Abstract*—A new current-mode bandgap reference circuit (BGR) which is capable of generating sub-1-V output voltage is presented. It has not only the lowest theoretical minimum current consumption among published current-mode BGRs, but also additional advantages of an inherent curvature-compensation function and not requiring NPN BJTs. The curvature-compensation is achieved by utilizing the exponential behavior of sub-threshold CMOS transistors to compensate the BJT base-emitter voltage high-order temperature dependence. By taking advantages of the continuing development of CMOS technology, sub-μW power consumption is achieved with a reasonable core area. Related design considerations and challenges are discussed and analyzed. The proposed BGR is realized in a TSMC 90 nm process. Measurement results shows a temperature coefficient without trimming as low as 10.1 ppm/°C over a temperature range of 70°C because of the proposed curvature-compensation technique. The average value is 32.6 ppm/°C which could be improved by trimming resistor ratios. The average power consumption at room temperature is 576 nW, with a core area of only 0.028 mm^2.**

***Index Terms*—Bandgap reference, nano-meter (nm), CMOS, low-power, curvature-compensation, nano-watt (nW), wireless sensor network**

I. Introduction

BANDGAP reference circuits (BGR) generate precise reference signals which are insensitive to process, voltage and temperature variations and have been used for decades because of their reliability. One of the major BGR design parameters is temperature coefficient (TC). For CMOS BGRs, this non-ideality is mainly due to the high-order temperature dependence of BJT base-emitter voltage (V_{BE}). Different curvature-compensation techniques have been developed, for example [1]–[9] etc. In [1] and [2], a non-linear current, which is generated by using an extra BJT, is applied to compensate the high-order temperature dependence. Piecewise-linear curvature-compensation technique has been proposed in [3] and adopted in [4]–[7], a CMOS non-linear current source is turned on and added to the output when the operating temperature is higher than a pre-determined value. As a result, the second-order behavior is corrected and the TC performance is improved by extending the temperature range. In [8], two current-mode BGRs, one of them using PNP BJTs and the other one using NPN BJTs, are constructed. Because they have similar temperature dependence, a second-order curvature-compensation can be achieved by subtracting their output current with a proper scale. Most curvature-compensation techniques require additional components and power consumption. A remarkable exception is [9], the BGR high-order temperature dependence is compensated by incorporating two different types of resistor whose first-order TCs are of opposite sign. Nevertheless intensive trimming may be needed to match the resistor ratios because the resistors are with different types. More curvature-compensation techniques and related discussion can be found in [10].

Another consideration is the power consumption. Sub-μW, or even lower, power consumption is targeted for power-aware applications such as medical devices and wireless sensor networks [11]–[14]. However only a few sub-μW BGRs can be found in literature [13]–[16]. This is because most BGRs contain resistors for voltage-to-current (V-to-I) conversion and/or vice versa, large resistance is needed in order to achieve such power consumption level. This can increase the chip area substansiously. As a result, some research [17]–[19] has been conducted on non-bandgap CMOS-only reference circuits which generate the output voltage based on MOS transistor threshold voltage (V_{TH}). The trade-off is a relatively large output error due to process variations [17], for example a coefficient of variation of 4 % is measured in [18] which is worse than that for BGRs (around 1 % in [14] and [20]). This is because the V_{TH} variation over process corners can be as large as $\pm$15 %, while the bandgap voltage variation is usually within $\pm$1 %. Trimming could be used to improve this error, but is undesirable due to increased area, cost and testing time.

The minimum width of resistors scales down with the continuing aggressive development of CMOS technology. Mega-ohm resistors can be realized with a reasonable area in state-of-the-art CMOS processes, hence sub-μW BGR power consumption is now achievable. For example the high-resistance poly resistor without salicide in the 90 nm CMOS process used in this work, its resistivity can be as large as 0.16 MΩ per 100 μm^2 and would increase even more favorably with more modern technology nodes. The drawbacks are the need of an extra salicide-blocking mask and, hence, increased fabrication cost. The resistor area is now less dominating, and becomes comparable to other components for BGR design.

In this work, a new current-mode BGR topology with an inherent curvature-compensation property is proposed. By

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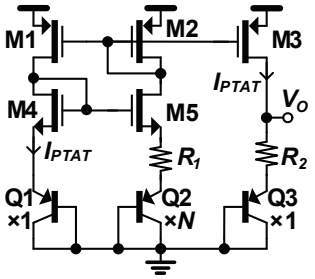


Fig. 1. A conventional voltage-mode BGR.

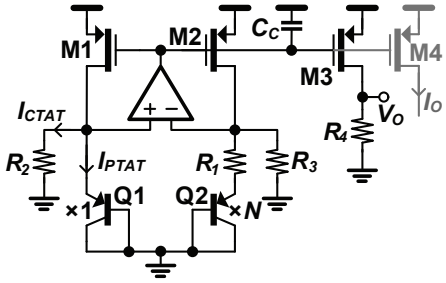


Fig. 2. The current-mode BGR proposed by Banba *et al.*

taking advantages of technology scaling, high-precision, low-power and small-area BGRs become flexible in modern nm CMOS technology. While MOS transistors do not benefit much in analog circuit design from the scaling, non-idealities such as short channel effects and gate leakage become even more problematic. BGR design in nm CMOS technology is studied. A proof-of-concept prototype is realized in a TSMC 90 nm CMOS process and shows good results.

This paper is organized as follows. Challenges and design issues of implementing BGRs in modern nm CMOS processes are discussed in Section II. Section III analyzes the proposed BGR and curvature-compensation technique. Verifications of the proposed BGR and discussion are presented in Section IV. Section V concludes the paper.

II. BGR Design in nm CMOS Processes

A. Basic BGR topologies

Fig. 1 shows a widely-used BGR structure. It can be shown that

$$V_O = V_{EB1} + n\ln(N)\frac{R_2}{R_1}\cdot V_T \tag{1}$$

where n is the diode non-ideal factor, N is the ratio between Q1 and Q2, V_T is the thermal voltage $\frac{kT}{q}$, k is Boltzmann constant, T is the absolute temperature, and q is the elementary charge of an electron. V_T is a proportional-to-absolute-temperature (PTAT) parameter with TC of approximately 85 μV/°C, on the contrary V_{EB} (or V_{BE} for NPN BJTs) is a complementary-to-absolute-temperature (CTAT) parameter with TC of approximately –1.6 mV/°C [21]. If we ignore high-order effects, V_O can be set to be first-order temperature-independent by sizing N and the ratio between R_1 and R_2 such that

$$M = n\ln(N)\frac{R_2}{R_1} = \left|\frac{\frac{\Delta V_{EB}}{\Delta T}}{\frac{\Delta V_T}{\Delta T}}\right| = \left|\frac{-1.6\text{ mV/°C}}{85\text{ μV/°C}}\right| \approx 19 \tag{2}$$

The output voltage is fixed to be approximately 1.2 V due to the silicon bandgap voltage, this limits the usability of this BGR in modern nm CMOS processes which are targeted to operate at low supply voltage.

To achieve sub-1-V output voltage, current-mode BGRs can be used [1]–[8] [13] [22]. Most of them are based on the structure proposed by Banba *et al.* [22]. The schematic is shown in Fig. 2. The idea is to convert both V_{EB} and V_T into current form and sum them with a proper scale. V_O is then given as

$$V_O = \frac{R_4}{R_2}V_{EB1} + n\ln(N)\frac{R_4}{R_1}V_T \tag{3}$$

The drawbacks are the additional components required and larger resistance for the V-to-I conversions. Current-mode BGRs also have the benefits of generating temperature insensitive reference current and multiple reference voltage (by replacing the output resistor with voltage dividers with the same total resistance) which may be required for large system designs [13].

One interesting variant is proposed in [5] and [13], the PTAT and CTAT current are generated independently. By scaling and summing them properly, reference current with desired TC can be generated and applied to design temperature-compensated circuits and temperature sensors [13].

B. Uses of NPN BJTs

In deep sub-μm CMOS processes, deep N-well layer is normally available. This enables the design of vertical NPN BJTs with moderate current gain ($\beta > 4$). Note that β is a PTAT parameter and can vary for 30 % due to process variations, the design may be more complicated if β is not large enough to ignore its effect. Some examples of CMOS BGRs using NPN BJTs can be found in [6] and [13]. However, unlike the BGRs shown in Fig. 1 and 2, the collector inputs of the NPN BJTs are not connected together in those structures, which potentially requires more area. Furthermore, because of the thickness of the deep N-well, the minimum size and spacing of NPN BJTs are usually larger than those of PNP BJTs for the same emitter area [15].

C. Line sensitivity

Line sensitivity is a very important BGR design parameter, it measures the sensitivity of the output voltage (or current) to the supply voltage and indicates the low-frequency power supply rejection ratio (PSRR). It is mainly limited by the finite output resistance of current mirrors, hence very long transistors [18] or advanced current mirror structures [19] [20] are required for high-performance reference circuits. The situation is even worse in nm CMOS processes because of the halo implant, which is commonly introduced in modern CMOS technology to reduce drain-induced barrier lowering effect for short channel length CMOS transistors. However it causes a severe degradation of the output resistance for longer channel lengths [23].

Regarding the current mirror structures, normal cascode, regulated cascode [20] and gain-boosted [5] [22] topologies

are widely used. The first two structures increase the headroom overhead and the latter one can only be applied to current mirrors with two branches.

D. Process variations

One very important feature of the BGRs shown in Fig. 1 and 2 is that, to the first order, their output voltage relies only on relative size ratios between components (resistors and BJTs), but not their absolute values. Hence very good matching (mismatch can be as small as 0.1 %) can be achieved by careful layout and the size constraints are reduced significantly.

However, equations (1) and (3) do not account for the transistor mismatch of the current mirrors. The current mismatch for transistors in strong inversion is usually modeled as [24]

$$\sigma^2_{\frac{\delta I_D}{I_D}} = \left(\frac{g_m}{I_D}\right)^2 \frac{A^2_{V_{TH}}}{WL} + \frac{A^2_K}{WL} \tag{4}$$

where $A_{V_{TH}}$ and A_K are the proportionality constants of the threshold voltage and mobility respectively, W and L are the transistor width and length respectively[1]. The first term is usually dominating. Small $\frac{g_m}{I_D}$ (i.e. large overdrive voltage) is preferred, but it is difficult in nm CMOS design due to the limited headroom.

Large transistors would be used instead, with a trade-off of poor high-frequency PSRR due to large parasitic capacitance. Moreover, this may cause gate leakage depending on the gate oxide thickness (t_{ox}). We do not see significant gate leakage effect in the 90 nm CMOS process used in this work. However it has been reported in [26] that if $t_{ox} \leq$ 1.7 nm, the gate leakage current density can be larger than 1 mA/cm^2 even with small gate-source voltage ($<$ 250 mV). There may exist a trade-off between the gate leakage and transistor matching for such processes.

III. Proposed Bandgap Reference Circuit

In this section, the proposed BGR and curvature-compensation technique are verified. So far, we assume the CTAT source V_{EB} is only first-order temperature-dependent which is not true in reality. Including the higher-order effect, V_{EB} can be written as [5] [27]

$$V_{EB}(T) = V_{BG}(T_R) - \frac{T}{T_R}\left[V_{EB}(T_R) - V_{BG}(T_R)\right] + (\eta - \zeta)V_T \ln\frac{T_R}{T} \tag{5}$$

where V_{BG} is the bandgap voltage of silicon extrapolated to 0 K, T_R is the reference temperature, η is a temperature constant depends on the technology with the most representative value 3.54, and ζ is the order of temperature dependence of collector current. The higher-order temperature dependence limits TC of first-order BGRs to be around 15 ppm/°C over a temperature range of 70°C (see Appendix I), curvature-compensation is required in order to achieve a better TC.

[1]Notice that the mismatch model is more complicated for sub-threshold transistors [25] and it is difficult to apply for hand calculations, hence it is not discussed in this work.

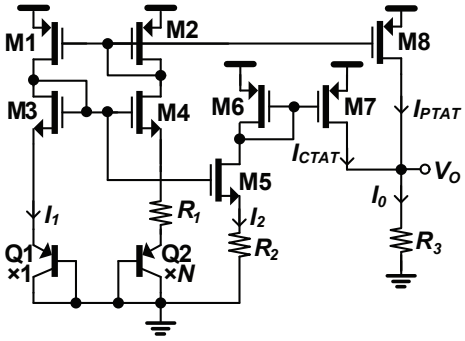


Fig. 3. The proposed BGR.

The basic concept of the proposed curvature compensation-technique is to generate a nonlinear voltage V_{NL} with high-order temperature dependence of approximately $-V_T(\eta - 1)\ln\frac{T_R}{T}$ by utilizing the exponential behavior of sub-threshold CMOS transistors, meanwhile the high-order temperature dependence of V_{BE} is $V_T(\eta-1)\ln\frac{T_R}{T}$ as shown later. V_{NL} and V_{BE} are summed in current form to perform the curvature-compensation. Similar solutions have been proposed in [1] and [2], however the proposed BGR has lower circuit complexity and current consumption. The idea is shown in Fig. 3 and the following conditions are assumed to be valid:

- All the NMOS transistors operate in the sub-threshold region and are saturated ($V_{DS} \gg V_T$). Their drain current is then given by

$$I_D \approx \mu C_{ox} V_T^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right) \tag{6}$$

  where μ is the electron mobility, C_{ox} is the oxide capacitance per unit area, V_{GS} is the transistor gate-source voltage, and m is the transistor sub-threshold slope parameter.
- The PTAT current (I_1) is first-order temperature-dependent and its higher-order temperature dependence can be ignored. Hence $\zeta = 1$ and I_1 can be written as

$$I_1 = \frac{k \cdot n\ln(N)}{R_1 q} T \tag{7}$$

- The high-order temperature dependence of the CTAT current (I_2), which is generated from V_{EB1}, is compensated. More details of the temperature compensation will be shown later in this section. Thus I_2 is also first-order temperature-dependent.
- $I_0 = I_1 + I_2$ and I_0 is constant at all temperature, in other words $\frac{\Delta I_1}{\Delta T} = -\frac{\Delta I_2}{\Delta T}$.
- I_1 and I_2 intersect at T_R. At $T = T_R$,

$$I_1(T_R) = I_2(T_R) = \frac{k \cdot n\ln(N)}{R_1 q} T_R \tag{8}$$

  Hence I_0 can be expressed as

$$I_0 = 2 \cdot I_1(T_R) = \frac{2k \cdot n\ln(N)}{R_1 q} T_R \tag{9}$$

  The situation is illustrated in Fig. 4.
- Short-channel effects of the MOS transistors and temperature-dependence of the resistors are negligible.

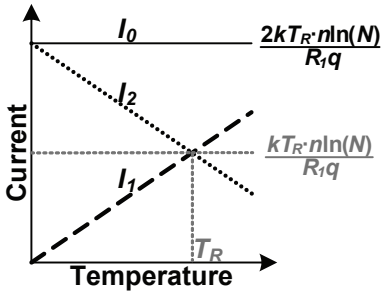


Fig. 4. I_{PTAT} (I_1), I_{CTAT} (I_2), and curvature-compensated current output (I_0).

It can be observed that

$$V_{EB1} + V_{GS3} = V_{GS5} + I_2 R_2 \tag{10}$$

Assume all NMOS transistors have the same size and V_{TH}, we have

$$I_2 = \frac{1}{R_2} V_{EB1} + \frac{1}{R_2} \overbrace{\left(m V_T \ln \frac{I_1}{I_2} \right)}^{V_{NL}} \tag{11}$$

$$= \frac{1}{R_2} \left\{ V_{BG}(T_R) - \overbrace{\frac{T}{T_R}[V_{EB}(T_R) - V_{BG}(T_R)]}^{\text{First-order terms}} + \overbrace{V_T \left[(\eta - 1) \ln \frac{T_R}{T} - m \ln \frac{I_2}{I_1} \right]}^{\text{Higher-order terms}} \right\} \tag{12}$$

By using Talyor series, if $x \approx 1$, $\ln(x) \approx x - 1$. This implies if both $\frac{I_1}{I_2}$ and $\frac{T_R}{T}$ are approximately equal to one within a certain range of temperature, the higher-order terms can be written as:

$$I_{2,HO} = \frac{V_T}{R_2} \left[-m \ln \frac{I_2}{I_1} + (\eta - 1) \ln \frac{T_R}{T} \right] \tag{13}$$

$$\approx \frac{V_T}{R_2} \left[-m \left(\frac{I_2}{I_1} - 1 \right) + (\eta - 1) \left(\frac{T_R}{T} - 1 \right) \right] \tag{14}$$

$$= \frac{V_T}{R_2} \left[-m \frac{I_0 - I_1}{I_1} + (\eta - 1) \frac{T_R}{T} + 1 - \eta + m \right] \tag{15}$$

Substitute (7) and (9) into (15),

$$I_{2,HO} = \frac{V_T}{R_2} \left[-m \frac{2T_R - T}{T} + (\eta - 1) \frac{T_R}{T} + 1 - \eta + m \right] \tag{16}$$

$$= \frac{V_T}{R_2} \left[(\eta - 1 - 2m) \frac{T_R}{T} - (\eta - 1 - 2m) \right] \tag{17}$$

m normally ranges from 1.1 to 1.5, the higher-order terms are now compensated and become almost zero. As a result,

$$I_2 \approx \frac{1}{R_2} \left\{ V_{BG}(T_R) - \frac{T}{T_R} [V_{EB}(T_R) - V_{BG}(T_R)] \right\} \tag{18}$$

Thus V_O can be found as

$$V_O = R_3 (I_1 + I_2) \tag{19}$$

$$= \frac{R_3}{R_2} \left\{ V_{BG}(T_R) - \frac{T}{T_R} [V_{EB}(T_R) - V_{BG}(T_R)] + \frac{R_2}{R_1} \frac{k \cdot n \ln(N)}{q} T \right\} \tag{20}$$

And the first-order temperature-dependence can be cancelled out by setting $\frac{R_2}{R_1}$ to

$$\frac{R_2}{R_1} = \frac{q [V_{EB}(T_R) - V_{BG}(T_R)]}{k \cdot n \ln(N) T_R} \tag{21}$$

and V_O becomes

$$V_O = \frac{R_3}{R_2} \cdot V_{BG}(T_R) \tag{22}$$

The proposed curvature-compensation technique is simple and requires no additional current consumption. To the best of the authors' knowledge, the BGR topology used in [13] and [15] has the lowest theoretical minimum current consumption among all current-mode BGRs and is given as

$$I_{min} = 3 \cdot I_{PTAT} + 2 \cdot I_{CTAT} = \frac{n \ln(N)}{R_{PTAT}} \left(3 V_T + 2 \frac{V_{EB}}{M} \right) \tag{23}$$

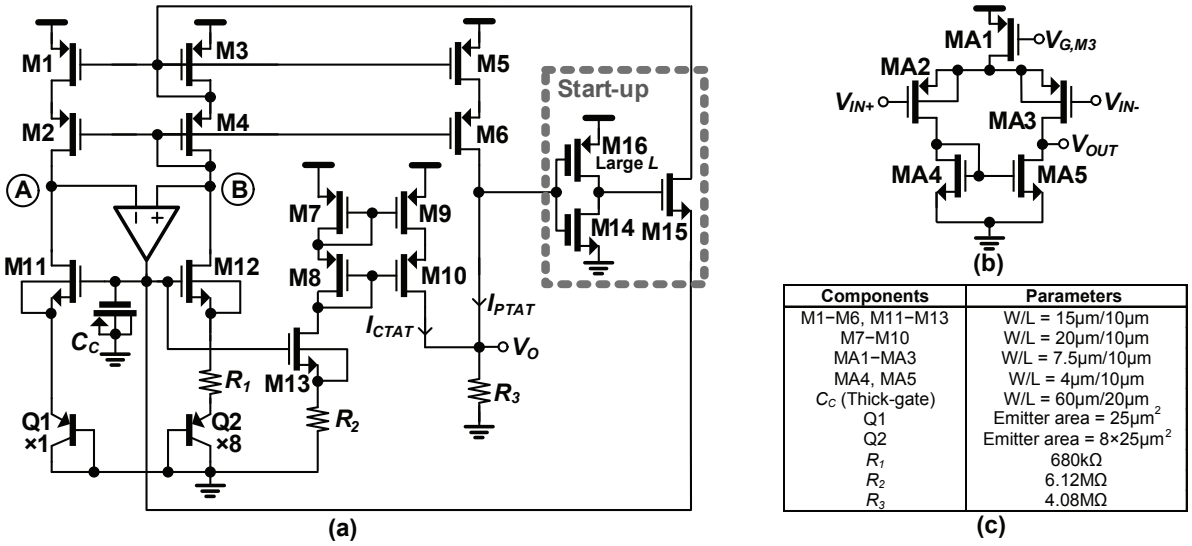
where R_{PTAT} is the resistor used in the PTAT current generator (for example R_1 in Fig. 1, 2 and 3). The proposed BGR achieves the same figure but with an additional curvature-compensation function and without using NPN BJTs.

So far we assume the short-channel effects of the MOS transistors and temperature-dependence of the resistors are negligible, however this is not valid in reality. The transistors short-channel effects may cause mismatches between current mirror branches which induce output offsets and degrade TC performance. The temperature-dependence of R_3 introduces another PTAT/CTAT parameter which needs to be compensated by adjusting the TC of I_0. As a result, I_0 is not temperature independent as assumed, instead it has a similar temperature dependence (but of opposite sign) as R_3. The first-order TC of the high-resistance poly resistor used in this work is approximately –0.02 % (200 ppm/°C).

IV. Verifications

A. Post-layout simulation results

The proposed BGR is designed in a TSMC 90 nm CMOS process and the schematic including start-up circuit is shown in Fig. 5. The supply voltage is 1.2 V. Assume a current mirror with 100 nA output, in order to achieve a line sensitivity of 0.1 %/V, an output resistance of 10 GΩ ($\frac{1\text{ V}}{0.1\ \% \cdot 100\text{ nA}}$) is required. Advanced current mirror structures are needed to achieve such large output resistance. Normal cascode, instead of gain-boosted, PMOS current mirrors are adopted because the current mirror containing M1–M6 has more than two branches, the trade-off is larger required voltage headroom which may reduce the operating temperature range. This is because V_{EB} and V_{TH} become too large at low temperature. Using thick-gate transistors can enable larger supply voltage



Components	Parameters
M1−M6, M11−M13	W/L = 15μm/10μm
M7−M10	W/L = 20μm/10μm
MA1−MA3	W/L = 7.5μm/10μm
MA4, MA5	W/L = 4μm/10μm
C_C (Thick-gate)	W/L = 60μm/20μm
Q1	Emitter area = 25μm^2
Q2	Emitter area = 8×25μm^2
R_1	680kΩ
R_2	6.12MΩ
R_3	4.08MΩ

(c)

Fig. 5. (a) The designed BGR, (b) OTA and (c) component parameters.

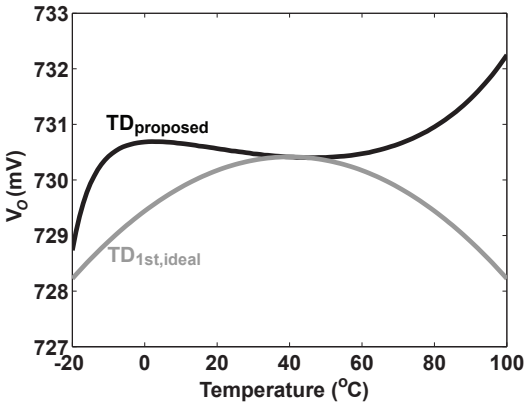


Fig. 6. $TD_{proposed}$ and $TD_{1st,ideal}$.

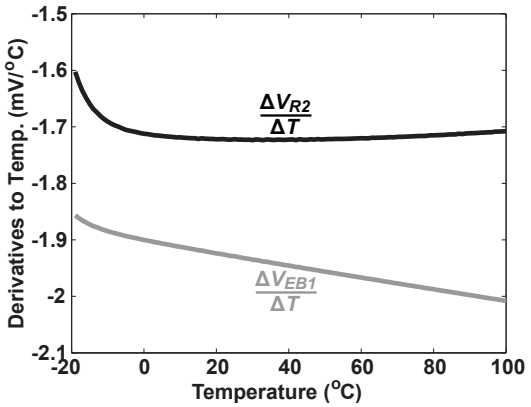


Fig. 7. $\frac{\Delta V_{R2}}{\Delta T}$ and $\frac{\Delta V_{EB1}}{\Delta T}$.

and, hence, wider operating temperature range, however such kind of transistors is usually not well-modeled and their larger V_{TH} increases the required supply voltage. To further improve the line sensitivity performance, an operational transconductance amplifier (OTA) is added to make the voltage at nodes A and B to be approximately the same. A compensation capacitor C_C of approximately 5 pF is added to improve the stability with a trade-off of longer start-up time. The NMOS transistors are put inside a deep N-well with their own substrate connected to their source, this improves the matching between their V_{TH}. All the transistors are with low-V_{TH} type and operating in sub-threshold region to minimize the required voltage headroom.

Fig. 6 depicts the post-layout simulated temperature dependence of the proposed BGR at the typical design corner ($TD_{proposed}$) and the temperature dependence of an ideal first-order BGR with the theoretical minimum second-order nonlinearity modeled by using (27) ($TD_{1st,ideal}$). The proposed BGR achieves an excellent TC of 5.5 ppm/°C over the commercial temperature range (0 to 70°C) and outperforms the ideal first-order BGR because of the proposed curvature-compensation technique. The TC performance outside this temperature range degrades due to the limited voltage headroom and the fact that the Taylor series assumption we made in Section III and the curvature-compensation do not hold anymore. The curvature-compensation effect can also be proved by comparing $\frac{\Delta V_{R2}}{\Delta T}$ (where $V_{R2} = I_{CTAT}R_2$) and $\frac{\Delta V_{EB1}}{\Delta T}$, with the post-layout simulation results at the typical design corner shown in Fig. 7. From 0 to 70°C, $\frac{\Delta V_{EB1}}{\Delta T}$ drops around 4 %, while $\frac{\Delta V_{R2}}{\Delta T}$ varies around 0.6 % only. The post-layout simulated noise density without any decoupling capacitor at 100 Hz is 680 nV/$\sqrt{\text{Hz}}$.

To analyze the BGR sensitivity to process variations and mismatches, 100 runs of post-layout Monte Carlo simulations are performed and the results are shown in Fig. 8. Fig. 8a depicts $\frac{\Delta V_{R2}}{\Delta T}$ versus temperature. $\frac{\Delta V_{R2}}{\Delta T}$ increases at low temperature for some runs because of the limited voltage headroom. The TC performance over the commercial temperature range is shown in Fig. 8b. 42 out of 100 runs achieve a TC of less than 15.1 ppm/°C and the minimum is 4.4 ppm/°C. The mean is 25.3 ppm/°C. The TC performance over a temperature range of 100°C (0 to 100°C) is shown in Fig. 8c. The mean

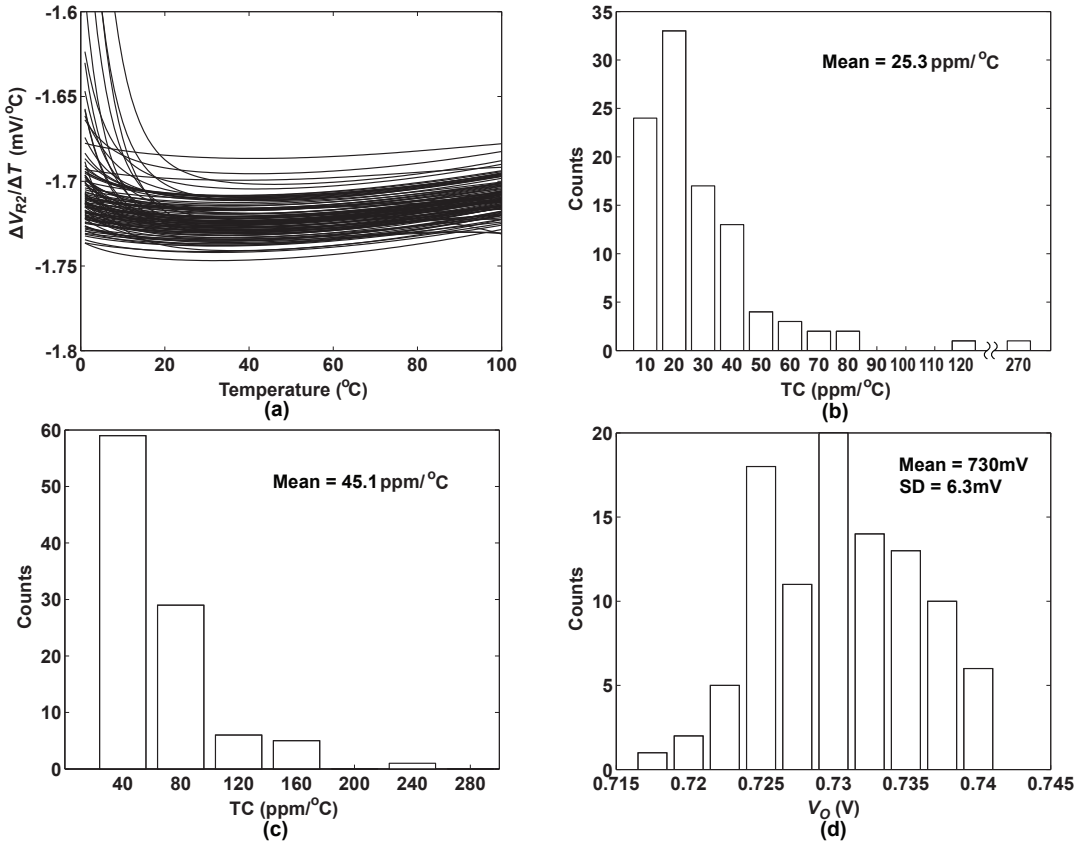


Fig. 8. Monte Carlo simulation results. (a) $\frac{\Delta V_{R2}}{\Delta T}$, (b) TC (0 to 70°C), (c) TC (0 to 100°C), and (d) V_O.

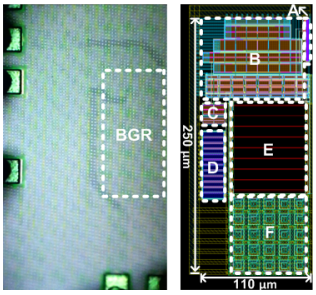


Fig. 9. (Left) A chip microphoto. (Right) The BGR layout: A: Start-up circuit; B: CMOS transistors; C: OTA; D: C_C; E: Resistors; F: BJTs and dummies.

TABLE I
MEASURED TEMPERATURE COEFFICIENT AND OUTPUT VOLTAGE OF FIVE SAMPLE CHIPS.

Sample	TC (10 to 80°C) (ppm/°C)	TC (0 to 100°C) (ppm/°C)	V_O at 30°C (mV)
I	15.8	43.5	712
II	10.1	45.3	725
III	43.5	55.8	729
IV	38.5	60.7	714
V	55	60.2	734
Mean (mV)	32.6	53.1	723
SD (mV)	N/A	N/A	9.4

is 45.1 ppm/°C, the degradation is due to the reasons mentioned above. Note that the TC performance is not Gaussian distributed, hence it is not meaningful to calculate its standard deviation (SD). Fig. 8d depicts V_O at room temperature, the mean and SD are 730 mV and 6.3 mV respectively which corresponds a coefficient of variation ($= \frac{\text{SD}}{\text{mean}}$) of 0.86 %.

B. Experimental results

A proof-of-concept prototype is fabricated and packaged in a JLCC64 package. A chip microphoto and the BGR layout are shown in Fig. 9. The core area is 0.028 mm^2. Five sample chips are measured without trimming and the results are presented in Table I and Fig. 10, the mean of V_O at 30°C is 723 mV with a coefficient of variation of 1.3 %. Sample II has the best overall performance. It achieves a TC of 10.1 ppm/°C over a temperature range of 70°C (10 to 80°C), which is lower than the theoretical minimum TC of first-order BGRs (15.1 ppm/°C) and proves the proposed curvature-compensation technique. We assume the variation to the targeted temperature range (0 to 70°C) is due to the process data mismatch. The average TC over the whole measured temperature range (0 to 100°C) is 53.1 ppm/°C which is still competitive to other sub-μW BGRs [14]–[16]. The average power consumption (including start-up circuit) with a 1.2 V supply at room temperature is 576 nW and the worst-case is 640 nW at 100°C.

Fig. 11 depicts the measured and post-layout simulated PSRRs, the line sensitivity which is indicated by the measured low-frequency PSRR is approximately 0.3 %/V. MOS transis-

TABLE II
A COMPARISON BETWEEN THE DESIGNED BGR AND OTHER PUBLISHED STATE-OF-THE-ART REFERENCE CIRCUITS.

		This Work		Sub-μW BGRs [14]	Sub-μW BGRs [15]	Curvature-compensated BGRs [2]	Curvature-compensated BGRs [6]	Curvature-compensated BGRs [9]	Non-BG reference circuits [17]	Non-BG reference circuits [18]	Non-BG reference circuits [28]
Curvature-compensated		Yes		No	No	Yes	Yes	Yes	No	No	No
Technology		90 nm CMOS		0.18 µm CMOS	90 nm CMOS	0.8 µm BiCMOS	0.13 µm CMOS	0.6 µm CMOS	0.35 µm CMOS	0.18 µm CMOS	0.13 µm CMOS
Min. supply voltage (V)		1.15		0.7	1.05	1	0.9	2	0.9	0.45	0.5
Power consumption (μW)		0.58		0.053	0.32	92	3.9	46	0.036	0.0032	0.0000022
Temp. range (°C)		10 to 80	0 to 100	–40 to 120	0 to 70	0 to 80	–50 to 150	0 to 100	0 to 80	0 to 125	–20 to 80
TC (ppm/°C)	Best	10.1	43.5	N/A	47.1	7.5	5.69	5.3	10	39	16.9
	Average	32.6	53.1	114	N/A	N/A	N/A	N/A	N/A	142	62
Output voltage (V)		0.72		0.55	N/A[a]	0.54	0.62	1.14	0.67	0.26	0.17
Line sensitivity (%/V)		0.3		≈0.16[b]	0.7	0.021	0.01	0.13	0.27	0.44	0.03
Area (mm^2)		0.028		0.025	0.026	3	0.1	0.057	0.045	0.043	0.001
Coefficient of variation (%)		0.86 (simulated) 1.3 (measured)		1.05	N/A	N/A	0.11	N/A	3.1	3.9	0.74
Multiple reference signals		Yes		No	Yes	Yes	Yes	No	No	No	No
Trimming		No		No	No	Yes	Yes	Yes	No	No	No

[a] Current reference of 90 nA output.
[b] Estimated from the low-frequency PSRR.

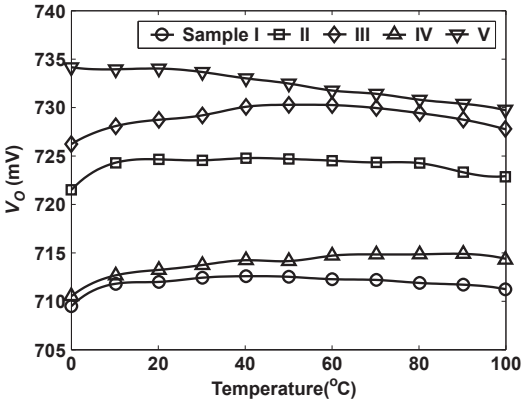


Fig. 10. Measured temperature dependence of all samples.

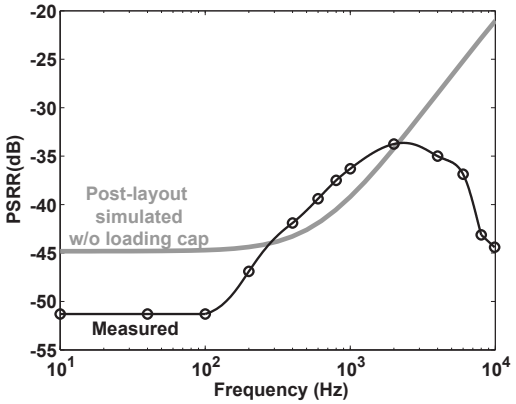


Fig. 11. Measured and post-layout simulated PSRRs.

tor output resistance is usually difficult to model precisely, this explains the 6 dB (2×) difference between the measured and post-layout simulated low-frequency PSRRs. The measured PSRR decreases at high frequency because of the parasitic capacitance of the package, bondwires and PCB etc. The characteristic of V_O versus supply voltage is shown in Fig. 12. The BGR starts to function properly when the supply voltage is higher than 1.15 V.

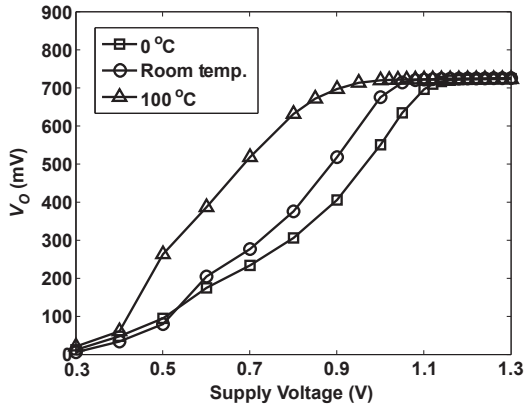


Fig. 12. Measured characteristics of V_O versus supply voltage.

The measured start-up time with a 10 pF probe loading is approximately 270 µs. Nevertheless the output parasitic components cannot be modeled accurately, hence the start-up behavior is not fully characterized. Instead, the start-up time is simulated with a 5 pF loading added and found to be 78 µs. Both PSRR and noise performance can be improved by adding decoupling capacitors with a trade-off of slower start-up.

C. Discussion

Table II shows a comparison between the designed BGR and other published state-of-the-art reference circuits. The area of the designed BGR is one of the smallest. It may not be a fair comparison since other designs may be using older CMOS technologies, however it proves the designed BGR takes advantages from the continuing development of CMOS technology and the possibility of implementing high-performance, low-power and small-area BGRs in modern nm CMOS processes. The relatively large line sensitivity is expected as a result of the lower transistor output resistance in nm CMOS processes as aforementioned. Both TC and coefficient of variation could be improved by trimming the resistor ratios [2] [6] with a trade-off of higher testing cost.

Compared to other sub-μW BGRs, the proposed BGR has the best TC performance. Although the BGRs in [14] and [16] are small-size and low-power because of their resistorless feature, they require relatively large number of transistors which may degrade the noise performance and cause a longer start-up time (6 ms is reported in [14]). The BGR in [15] uses NPN BJTs which is not preferred as the reasons mentioned in Section II.B. The designed BGR has the lowest power consumption compared to other curvature-compensated BGRs. The BGR in [6] utilizes the piecewise-linear curvature-compensation technique to extend the operating temperature range and improve the TC performance, similar techniques and/or trimming could be applied to the proposed BGR for improved performance.

Compared to the V_{TH}-based CMOS-only reference circuits in [17] and [18], the designed BGR shows a better coefficient of variation. Although they have very small power consumption, the $\pm 3\sigma$ output error due to process variations can be >18 % which limits their usability without trimming. A very interesting structure has been proposed in [28], it contains only two NMOS transistors with different V_{TH} and the output voltage is generated based on the V_{TH} difference. As a result, it is relatively less sensitive to process variations and pico-watt power consumption and small core area are achieved. However native transistor which is usually not accurately modeled is required, this may increase the design difficulty. For both V_{TH}- and ΔV_{TH}-based reference circuits, their output voltage relies on less fundamental parameters (for example, V_{TH} and μ etc.), relatively worse TC performance is expected [28].

Multiple reference voltage and/or current are usually required for large system designs. Unlike current-mode BGRs, CMOS-only reference circuits (including both bandgap and non-bandgap types) usually generate single reference voltage. Additional components (for example buffers, resistors and voltage dividers etc.), area and power consumption are required in order to do this.

V. Conclusion

A new sub-μW current-mode BGR has been presented. It has an inherent curvature-compensation property, together with the lowest theoretical minimum current consumption among published current-mode BGRs. A proof-of-concept prototype has been successfully implemented in a TSMC 90 nm CMOS process and shows competitive results, especially in terms of TC and power consumption. The measured TC without trimming is as low as 10.1 ppm/°C over a temperature range of 70°C, which is lower than the theoretical minimum TC of first-order BGRs and proves the proposed curvature-compensation technique. The average TC over an extended temperature range of 100°C is measured to be 53.1 ppm/°C which is competitive to other published sub-μW BGRs.

The measured average power consumption at room temperature is 576 nW, with a small core area of 0.028 mm^2. The mean of the measured output voltage at 30°C is 723 mV with a coefficient of variation of 1.3 %, which is good enough for many applications without trimming. Implementations of high-precision, low-power and small-area BGRs in state-of-the-art CMOS technology are proved to be possible. To the best of the authors' knowledge, the designed BGR is the only sub-μW curvature-compensated BGR that can be found in literature.

CMOS-only reference circuits may provide lower power consumption. Nevertheless, design trade-offs such as sensitivity to process variations, precision and flexibility etc. have to be considered as discussed. Thus, it remains an open question whether resistor-based BGRs or CMOS-only reference circuits will deliver ultimate performance, especially in modern nm CMOS processes.

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Appendix I

The theoretical minimum TC of the conventional BGR ($TC_{min,conv}$), which is shown in Fig. 1, over a certain temperature range (from T_L to T_H) is analyzed as follows. Consider only the first- and second-order TCs of V_{EB1} and assume all other higher-order effects are ignorable, V_{EB1} can be expressed as

$$V_{EB1} = V_{BG}(T_R) + a_1 T + a_2 T^2 \tag{24}$$

where a_1 and a_2 are the first- and second-order TCs respectively. Hence V_O is given as

$$V_O = V_{BG}(T_R) + a_1 T + a_2 T^2 + n \ln(N) \frac{R_2}{R_1} \cdot V_T \tag{25}$$

Because the conventional topology is first-order temperature-compensated, V_O becomes

$$V_O = V_{BG}(T_R) + a_2 T^2 \tag{26}$$

The best BGR TC can be obtained when T_R is set to the middle of the targeted temperature range, in other words $T_R = T_L + \frac{\Delta T}{2}$, where $\Delta T = T_H - T_L$. Then we can write $TC_{min,conv}$ as

$$TC_{min,conv} = \frac{|\Delta V_{O,min}|}{(\Delta T) V_{BG}(T_R)} = \frac{|a_2| \left(\frac{\Delta T}{2}\right)^2}{(\Delta T) V_{BG}(T_R)} \tag{27}$$

From Fig. 7, it can be observed that $a_2 \approx$ –1 µV/°C when $T \geq 0$°C. As a result, for the CMOS process used in this work, $TC_{min,conv}$ over temperature ranges of 70°C and 100°C are approximately 15.1 ppm/°C and 21 ppm/°C respectively. Similar analysis can be applied to other first-order BGRs and same results can be obtained.

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A.6 Paper-VI

K. K. Lee and T. S. Lande, "A wireless-powered IR-UWB transmitter for long-range passive RFID tags in 90 nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, to be published, DOI: 10.1109/TCSII.2014.2350292.

A Wireless-Powered IR-UWB Transmitter for Long-Range Passive RFID Tags in 90 nm CMOS

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***Abstract*—An impulse-radio ultra-wideband (IR-UWB) transmitter (TX) intended for long-range passive radio-frequency identification tags is presented. It is wirelessly powered by an ultra-high-frequency (UHF) signal. A 128-b pseudo-noise code is transmitted when enough energy is harvested. A new on-off-keying multi-cycle energy-efficient IR-UWB pulse generator (PG) is proposed, a co-design with power management circuits is introduced to improve the system supply noise performance. A novel injection-locking divider co-designed with RF voltage rectifier is proposed to eliminate the injection input resistive load which exists in some designs, otherwise the input sensitivity would be degraded. A proof-of-concept prototype is fabricated in a TSMC 90 nm CMOS process. Measurements show the TX input sensitivity to be approximately –17.5 dBm with a 900 MHz UHF input. The measured PG output swing is 195 $mV_{p\text{-}p}$ with a –10-dB bandwidth of approximately 3.4 GHz.**

***Index Terms*—Transmitter, RFID tag, UWB, pulse generator, injection locking frequency divider, wireless-powered, co-design**

I. Introduction

AFTER the Federal Communication Commission (FCC) released ultra-wideband (UWB) band for unlicensed uses, impulse-radio (IR) communication has been an active research topic. Compared to narrowband (NB) RF technologies, its pulsed nature makes it possible to construct energy-efficient transmitters (TX) and insensitive to fading. The large bandwidth (BW) provides higher data rate and good localization ability. Due to these advantages, research [1]–[4] has been conducted to apply IR-UWB technology for radio-frequency identification (RFID) applications which mainly rely on NB technologies nowadays. Different types of IR-UWB RFID tags and trade-offs can be found in [4]. Tags without battery (wireless-powered or chipless) are preferred because of the cost and product size considerations. Although wireless-powered IR-UWB tags have a higher cost than the chipless counterparts, they provides longer reading range and the possibility of embedding sensors and related circuits.

Battery-powered IR-UWB transceivers have been developed and showed very promising results. In [5], a large output-swing (6.4 $V_{p\text{-}p}$) pulse generator (PG) and a communication distance of 200 m has been demonstrated. Nevertheless wireless-powered IR-UWB tags in [1], [2] and [3] offer limited reading range (<1 m) due to the limited energy available and, hence, weak emission power on the tag side. To improve this, the data can be transmitted repeatedly, this introduces higher processing gain and averages out the noise, hence the signal-to-noise ratio (SNR) and reading range are increased. Note that the hand-shake protocols become complicated when there are large number of tags and amount of data in the system. This may increase the tag circuit complexity and energy consumption, hence the reading range is reduced. To solve this, a long-range passive UWB RFID system using a uni-directional communication scheme has been proposed in [6]. A wireless-powered IR-UWB TX for RFID tags in this system is implemented and presented in this work. IR-UWB technology makes the tags insensitive to fading and provides good localization ability. The uni-directional communication scheme eliminates the hand-shake protocols and pushes the circuit complexity to the reader side. Also novel IR-UWB PG and injection-locking frequency divider (ILD) structures are proposed for improved TX performance.

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II. Circuit Design

A. Top system

A block diagram of the RFID system is shown in Fig. 1, the TX contains four main blocks: power management unit (PMU), symbol generator, clock extractor and IR-UWB PG. The TX is operated in two modes: *(1) Energy-harvesting mode*: The TX harvests energy from an ultra-high-frequency (UHF) signal (around 900 MHz) sent from the reader. The energy is stored inside a 100 nF off-chip storing capacitor. Only the PMU is on during this period to minimize the power consumption and improve the input sensitivity, all the other blocks are in stand-by mode and draw leakage current only. *(2) Transmission mode*: When the stored energy is higher than a pre-determined threshold by monitoring the supply voltage, the TX sends out its own symbols containing 128-b length pseudo-noise (PN) codes. The clock signal is extracted from the UHF signal by using an ILD. The capacitor is discharged after transmission and the TX returns to energy-harvesting mode. More complex power-management schemes

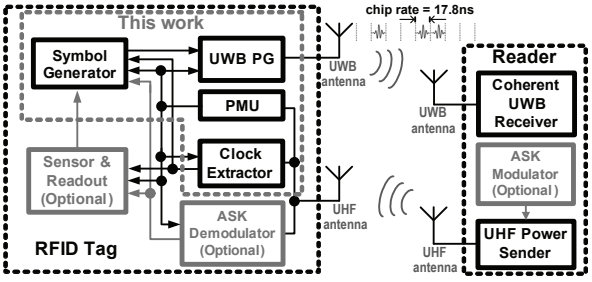

Fig. 1. Block diagram of the proposed RFID system.

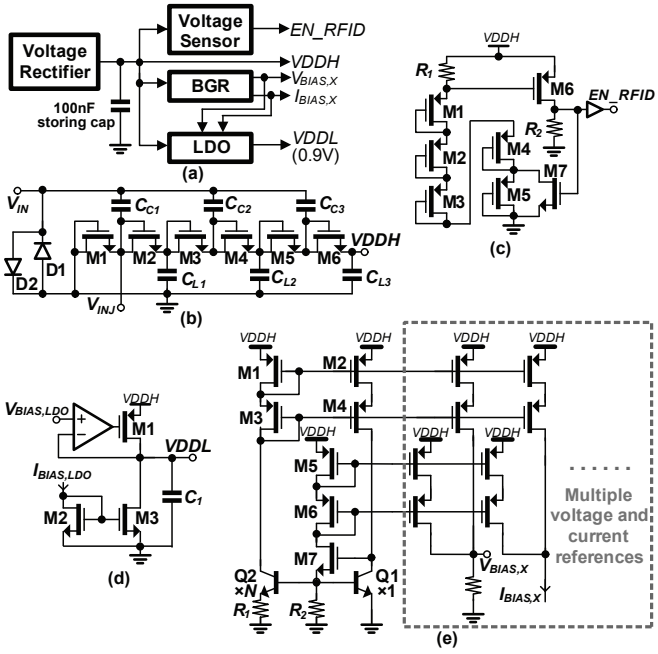

Fig. 2. (a) PMU, (b) voltage rectifier, (c) voltage sensor, (d) LDO, and (e) BGR.

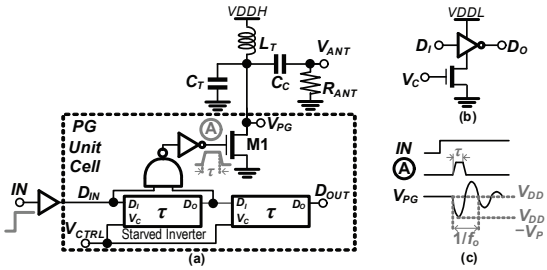

Fig. 3. (a) PG unit cell, (b) starved inverter, and (c) related operation.

and additional control circuits could be used to avoid the capacitor discharging, however this may increase the power consumption of the PMU and degrade the sensitivity.

The coherent UWB rake receiver (an example structure can be found in [7]) inside the reader continuously monitors incoming signals and compares them with the stored symbols using cross-correlation. The operations are repeated until sufficient SNR is achieved to detect the tags and the reader stops the energy supply. The channel separation is given by the system asynchronous code-division multiple access and inherent ALOHA properties [6]. Every tag needs different time to harvest energy due to process variation, component mismatch and distance to the reader etc., transmissions will be sufficiently distributed for acceptable interference, even with a large number of tags in operation.

Similar to other IR-UWB RFID systems [2] [3], amplitude-shift key (ASK) demodulator and modulator could be added to the system optionally to establish a bi-directional communication and add more functionalities. The trade-offs are more complicated hand-shake protocols, increased circuit complexity and reduced reading range.

B. PMU

Fig. 2a shows a block diagram of the PMU. The voltage rectifier harvests energy from an UHF antenna and stores the energy inside the storing capacitor. The voltage sensor monitors the rectifier output voltage (VDDH) and wakes up remaining circuits when VDDH is higher than a loosely-controlled threshold ($\approx$ 1.4 V). The ILD and delay-line inside the PG require stable and well-controlled supply voltage and reference current/voltage, which are achieved by using the bandgap reference (BGR) and low-dropout regulator (LDO).

The schematic of the voltage rectifier is shown in Fig. 2b, it is based on a 3-stage Dickson multiplier and constructed by native NMOS transistors with threshold voltage of around 200 mV. The diodes at the input limit the maximum input voltage and prevent the chip breaking down when too much energy is harvested. The voltage sensor is shown in Fig. 2c. The gate voltage of M6 is pulled up by R_1 until VDDH is high enough for the PMOS transistors to be on (i.e. VDDH $\geq 5 \cdot V_{THP} \approx$ 1.4 V, where V_{THP} is the threshold voltage of PMOS transistors). In order to provide fast transition, the voltage change is amplified by a common-source amplifier consisting of M6 and R_2. EN_RFID is then switched to '1', the TX enters transmission mode and all other blocks are enabled. Meanwhile, M7 is turned on and this generates a hysteresis width of one V_{THP}. The schematics of the LDO and BGR are shown in Fig. 2d and 2e respectively, a second supply voltage (VDDL) of approximately 0.9 V is generated to supply the clock extractor, symbol generator and the delay-line inside the PG. The BGR presented in [8] is used, with a line sensitivity of 0.8 %/V and a temperature coefficient of 47.1 ppm/°C over a temperature range of 70°C.

C. IR-UWB PG

The PG is usually the most energy-consuming component inside IR-UWB TXs and the tag reading range is proportional to its transmitted power. Moreover it needs to deliver large power to the antenna and the pulsed nature generates large high-frequency noise on the supply. It is challenging to design LDO for such high-power pulsed system. A new on-off-keying (OOK) PG structure is proposed to solve these problems.

The unit cell is shown in Fig. 3a. It works like a class-E RF power-amplifier with an a pulsed input and a similar approach has been adopted in [3]. The propagation delay (PD, with a length of τ) of a starved inverter (the schematic is shown in Fig. 3b) is used to generate a pulse with a width of approximately τ at node A and M1 is turned on. This pulls down the output voltage (V_{PG}) to $V_{DD} - V_P$ and injects energy into an RLC tank consisting of the UWB antenna resistance R_{ANT}, an on-chip inductor L_T and a capacitance C_T which includes tuning and parasitic capacitors. C_C is an off-chip coupling capacitor for measurement purposes only. The injected energy circulates back and forth inside the tank with its resonant frequency $f_o = (2\pi\sqrt{L_T C_T})^{-1}$ as shown in Fig. 3c. Due to the R_{ANT}, the signal decays as: $V_{PG} = V_{DD} - V_P \exp\left(-\frac{f_o}{Q_T}t\right)\sin(2\pi f_o t)$, where Q_T is quality factor (QF) of the tank and given as $Q_T = \frac{R_{ANT}}{\omega_o L_T} = \omega_o C_T R_{ANT}$. The signal dies out in approximately Q_T cycles.

One feature of the proposed PG is that the pulse width is scalable by adding more unit cells. If more unit cells are cascaded in series, more-cycle and higher-energy outputs can be generated. Two unit cells are cascaded with f_o and Q_T set to approximately 5 GHz and 2 respectively (the choices of f_o

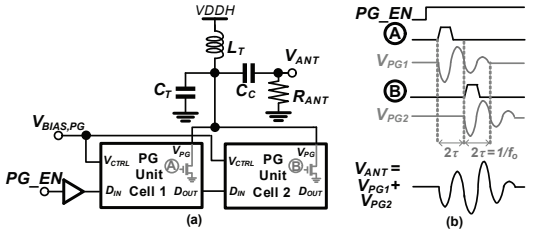

Fig. 4. (a) Proposed IR-UWB PG and (b) its operation.

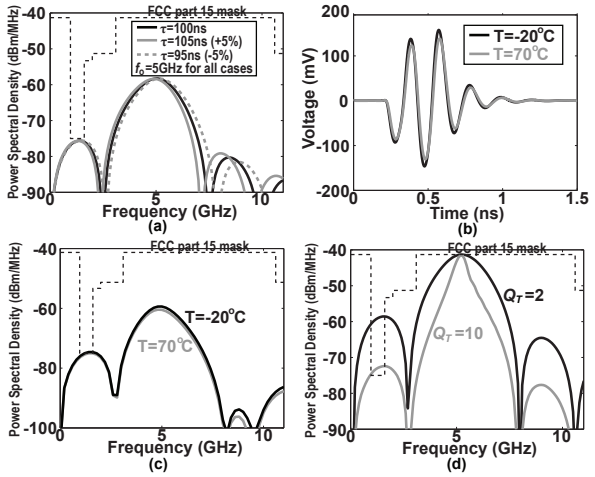

Fig. 5. (a) Simulated power spectra with different mismatches between 2τ & f_o^{-1}, (b) simulated PG output waveforms and (c) corresponding power spectra at different temperature and (d) simulated power spectra with different Q_T.

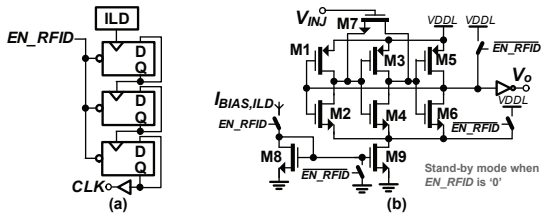

Fig. 6. (a) Clock extractor and (b) ILD.

and Q_T will be discussed later) in this design as shown in Fig. 4a, the idea is depicted in Fig. 4b. Note that the waveforms V_{PGi} (V_{PG1} and V_{PG2}, which are highlighted in grey color) represent the output signals contributed by the *i*-th unit cell, they are shown for illustration proposes and do not exist actually in the system. To minimize the influence from the supply voltage and process variations, VDDL is set to 0.9 V and $V_{BIAS,PG}$ is set adequately by trimming the BGR resistor ratios such that the unit cell PD and the period of the resonant signals are approximately the same (i.e. $2\tau \approx \frac{1}{f_o}$), the output signals from all unit cells are in phase and added together. Fig. 5a shows the system-level simulated power spectra with $\pm 5\%$ mismatches between 2τ and $\frac{1}{f_o}$, around $\pm 2\%$ variation on peak frequency and $\pm 2.5\%$ variation on BW are observed. Note that energy is concentrated at around f_o because of the tank bandpass property, this makes the PG less sensitive to the mismatch and temperature variation. Post-layout simulated PG waveforms and power spectra with 5 MHz pulse repetition frequency (PRF) at different temperatures are shown in Fig. 5b and 5c respectively.

There are some design trade-offs here. First, high signal frequencies (>6 GHz, which also imply higher f_o) would be less sensitive to the interference from existing radio systems like 802.11a. Nevertheless lower signal frequencies result lower propagation losses and circuit energy consumption. Since long reading range is one of the main goals of this work, the PG is targeted to operate at lower frequencies of the FCC mask. Attention should be paid to the interference issues for example using 802.11g instead of 802.11a for the radios nearby. Second, a narrow tank BW (large Q_T) provides larger attenuation on the low-frequency sidebands and makes the PG output fit the FCC mask better, however it may filter out the in-band energy and reduce the energy efficiency. Fig. 5d depicts the situation, increasing Q_T from 2 to 10 reduces the low-frequency sideband energy by 13.8 dB with a trade-off of smaller in-band energy. In addition, the data rate and localization ability improve with increased BW and Q_T has to be much smaller than the QF of other components so as to prevent insertion losses due to the parasitic components. The QF of on-chip spiral inductors is normally around 10–20. As a trade-off, Q_T is set to approximately 2 in the designed PG.

The output parasitic capacitance which is usually dominating inside the system is tuned out by L_T, the driving requirement and, hence, the transistors size of the output driver are reduced. In other words, the capacitive and switching losses are also reduced which makes the designed PG energy-efficient. Another advantage is that L_T connects the PG output to the VDDH at DC which provides electrostatic discharge protection.

The output driver drives a large instantaneous power to the antenna and is the main cause of the high-frequency supply noise. Supplying the output driver through the LDO is not a good idea because the high-frequency noise would couple to other circuits through the LDO. Also, LDOs which have fast-response to handle the impulse noise (i.e. good load regulation) would be power-demanding. Notice that the output driver of the proposed PG does not require a well-defined supply voltage, the DC variation only changes the emission power and it may be compensated by adjusting the processing gain. Post-layout simulations show the peak energy decreases for 0.7 dB when the supply voltage drops from 1.4 V to 1.1 V. As a result, the output driver is supplied by VDDH with the large storing capacitor providing good supply noise rejection.

D. Clock extractor

It is important that the reader and tags have the same chip rate for reliable symbol detection. Crystal oscillator or phase-locked loop could be used to generate precise clock signals, however long start-up time and, hence, large energy consumption are required due to the large QF of the crystal resonator. Instead ILD is adopted in this work because of high energy-efficiency. If the targeted output frequency is close to the ILD free-running oscillating frequency, the start-up time (including lock time) can be very short (a few clock cycles according to simulations). The trade-off is the relatively poor jitter performance.

A block diagram of the clock extractor is shown Fig 6a. It consists of a divide-by-2 (/2) ILD and three /2 digital dividers, giving a division ratio of 16 in total. The ILD is based on the structure proposed in [9], the schematic is shown in Fig. 6b. A novel co-design between the ILD and voltage rectifier is

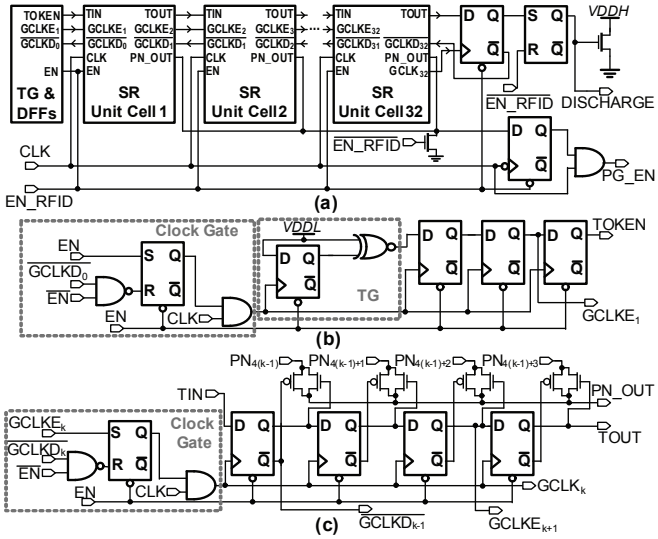

Fig. 7. (a) The symbol generator, (b) TG, and (c) SR unit cell.

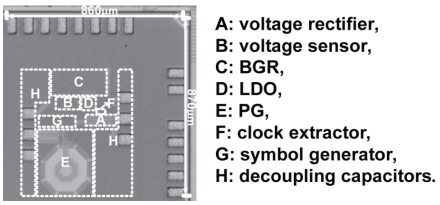

Fig. 8. Chip microphotograph.

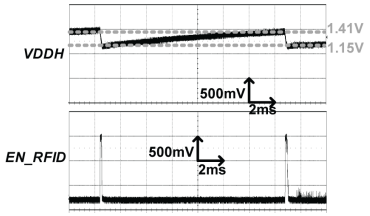

Fig. 9. Measured hysteresis behavior.

proposed. Unlike the ILDs for RFID tags in [3] and [10], the DC voltage of the injection input is biased by either resistors or diode-connected transistors which generate resistive loads to the antenna and degrade the sensitivity, the designed ILD draws the injection signal from the node V_{INJ} of the rectifier (see Fig. 2b) and introduces only a small capacitive load to the antenna. The DC voltage of V_{INJ} is approximately 240 mV ($\approx \frac{VDDH}{6}$ since the rectifier contains six diode-connected NMOS transistors) which is approximately the same as the threshold voltage of M7. As a result, M7 is switched on and off with the frequency of the injecting signal (f_{INJ}) and the output frequency is locked to $\frac{f_{INJ}}{2}$. Detailed analysis can be found in [9]. The digital dividers are implemented using true-single-phase-clock type D-flip-flops (DFF) providing small-area and low-power advantages.

E. Symbol generator

The structure of the symbol generator is illustrated in Fig. 7a. Each symbol is composed of a 128-b PN code which is assumed to be hard-coded. The token generator (TG) generates a token bit of one clock cycle width. The token bit is passed along a 128-b shift register (SR) and multiplexes out one bit of the PN code in sequence every cycle. The PG is enabled if the outputted signal (PG_EN) is '1'. Clock-gating is used to minimize the power consumption, the clock signal is delivered to maximum six DFFs only. The schematics of the TG and SR unit cell is shown in Fig. 7b and 7c respectively, the DFFs following the TG provides time for the clock signal start-up. One cycle after shifting out the whole PN code, DISCHARGE goes to '1' and VDDH is discharged until it reaches approximately 1.4 V$-V_{THP}$, then EN_RFID is disabled by the voltage sensor and the TX returns to energy-harvesting mode. The operations are repeated until the reader stops the energy supply (the UHF signal).

III. Experimental Results

A proof-of-concept prototype is implemented in a TSMC 90 nm CMOS process and a chip microphotograph is shown in Fig. 8. The chip area including pads is 0.75 mm^2. The UHF input signal frequency is 900 MHz. The tag starts to function properly when the input power is higher than –17.5 dBm, this would correspond a reading range of 12.6 m by using Friis transmission equation with 4 W EIRP radiation and 0 dB gain transmitting/receiving antenna. The measured maximum power consumption including leakage during energy-harvesting mode is 1.8 µW. The charging and transmission times are approximately 13 ms and 2.5 µs respectively. The hysteresis behavior is measured and shown in Fig. 9. When VDDH is higher than 1.41 V approximately, EN_RFID goes high and the TX starts transmitting. VDDH is then discharged after transmissions and the TX returns to energy-harvesting mode again when VDDH drops to 1.15 V approximately.

The detailed operation is depicted in Fig. 10a, both EN_RFID and CLK are outputted off-chip by output buffers with separated power supplies for testing purposes. The rectifier input and PG output are probed on chip. When EN_RFID goes high (notice that the slow rising edge is due to weak driving ability of the output buffer), the clock extractor starts up and the PG starts to transmit after the clock signal is settled. The PN code is set to '10100110'$\times$16 for demonstration and shifted out to trigger the PG.

A zoom-in version of the clock signal is shown in Fig. 10b. The swing is attenuated because the probe impedance decreases beyond 1 MHz and loads the output buffer, we assume the clock signal on-chip is still rail-to-rail. The cycle-to-cycle jitter is measured after the clock signal settled and shown in Fig. 10c, the peak-to-peak value and the standard deviation are 260 ps and 44 ps respectively. This jitter may be tolerated provided that processing gain is utilized [7]. The measured locking range (LR) with the minimium input power (–17.5 dBm) is approximately 260 MHz (800–1060 MHz). Simulations show that the LR reduces for 13% when the DC voltage of V_{INJ} decreases for 10%.

A zoom-in version of the PG output when VDDH = 1.41 V is shown in Fig. 10d, the output swing and pulse width with a 50 Ω loading are 195 mV$_{p\text{-}p}$ and 578 ps respectively. The corresponding power spectrum with 10 MHz PRF is shown in Fig. 10e, the –10-dB BW is 3.4 GHz (3.5–6.9 GHz) and the peak is –60.4 dBm/MHz. Adding highpass filters can reduce the low-frequency sideband energy and allow larger peak energy, the trade-offs are increased cost and energy

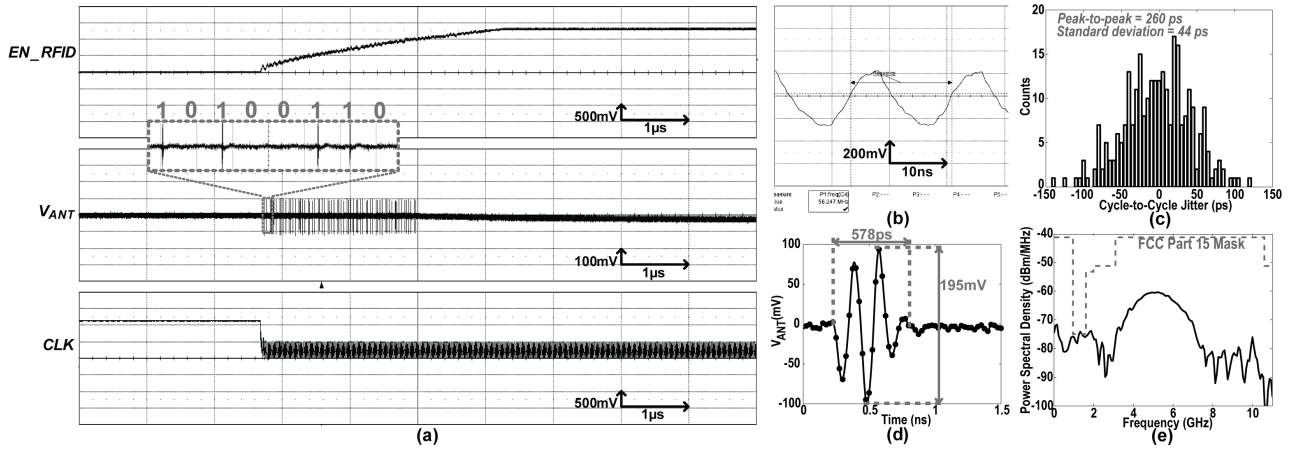

Fig. 10. (a) Measured transmission operation, (b) a zoom-in version of CLK, (c) a zoom-in version of V_{ANT}, (d) a histogram of the measured cycle-to-cycle jitter, and (e) measured power spectrum of the PG output.

consumption. It is difficult to measure the power consumption during transmission mode due to the multi-mode operation and small duty-cycle. Assume balanced PN code with equal number of '0' and '1', the post-layout simulated TX energy consumption during transmission is 7.2 pJ/b and around 76 % of this (5.5 pJ/b) is due to the IR-UWB PG. The post-layout simulated average power consumption of different blocks during transmission is shown in Table I.

Table II summarizes the design performance and compares it with other related works. The designed TX shows a competitive performance especially with respect to PG performance and energy consumption. Note that the design in [2] shows a very low energy consumption because of the lower PG transmitted energy, however not enough data (center frequency and –10-dB BW) is provided to make a fairer comparison.

TABLE I
POST-LAYOUT SIMULATED AVERAGE POWER CONSUMPTION OF DIFFERENT BLOCKS DURING TRANSMISSION.

	PG	Clock extrac.	Symb. gen.	LDO (incl. dropout loss)	Others
Power cons. (µW)	309	18	28	51	0.8

TABLE II
A COMPARISON WITH OTHER WIRELESS-POWERED IR-UWB TXS.

	[1]	[2]	[3]	This work
CMOS nodes (nm)	130	180	180	90
Modulation	OOK	BPSK	OOK	OOK
UHF input sensitiviy (dBm)	14	–19.4	–18.5	–17.5
PG output swing (mV_{p-p})	110	50	220[b]	195
PG center freq. (GHz)	7.9	N/A	N/A	5.2
PG –10-dB BW (GHz)	0.53	N/A	N/A	3.4
Energy consumption (pJ/b)	58[a]	1.66	N/A[c]	7.2 (sim.)
Chip area (mm^2)	4	4.5	4.5	0.75

[a] Energy consumption of the IR-UWB TX only. [b] Single decayed sine-wave output, the total output power is lower than the proposed TX. [c] With only the PG energy consumption of 9.2 pJ/b reported.

IV. CONCLUSION

A wireless-powered IR-UWB TX intended for long-range passive RFID tags has been presented. Combining IR-UWB technology with long symbols provides large number of tags with acceptable interference. Precise localization is feasible with elaborate receiver design [7]. A proof-of-concept prototype has been successfully implemented in a TSMC 90 nm CMOS process. The measured power consumption during energy-harvesting mode is only 1.8 µW, which results a good input sensitivity of –17.5 dBm. Combined with processing gain, long-range sensing can be provided. The proposed ILD co-designed with the RF voltage rectifier generates only a capacitive load to the antenna, hence the clock signal is locked to the targeted frequency even with such low input power. A new multi-cycle energy-efficient IR-UWB PG has been proposed, co-designing with PMU provides good supply noise management. A relatively large PG output swing of 195 mV_{p-p} is achieved even with a low TX energy consumption of 7.2 pJ/b.

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A.7 Paper-VII

K. K. Lee and T. S. Lande, "A 2.8–7.5 pJ/pulse highly-flexible impulse-radio ultra-wideband pulse-generator," preparing for publication.

A 2.8–7.5 pJ/Pulse Highly-Flexible Impulse-Radio Ultra-Wideband Pulse-Generator

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***Abstract*—A low-power on-off-keying impulse-radio (IR) ultra-wideband (UWB) pulse generator (PG) intended for wireless-powered IR-UWB radio applications is presented. The proposed PG has high flexibility, the center frequency, output power and pulse-width (PW) are controllable depending on channel conditions and data rates. Qualitative frequency-domain and transient analyses are presented. A new figure-of-merit (FoM) is proposed such that a more precise comparison between different PGs can be made. The PG is successfully implemented in a TSMC 90 nm CMOS process, measurements show the energy consumption and FoM to be 2.8–7.5 pJ/pulse and 1.6–2.6% respectively. The output swing and PW are 277–329 $mV_{p\text{-}p}$ and 509–1088 ps respectively. The core area is 0.092 mm^2.**

***Index Terms*—Impulse-radio (IR), ultra-wideband (UWB), CMOS, pulse generator, low-power, wireless-powered**

I. Introduction

Since the Federal Communication Commission (FCC) released a large spectral mask (i.e. 3.1–10.6 GHz) for unlicensed uses, ultra-wideband (UWB) technology has been an active research field. The wide spectral mask not only enables higher date rate, but also precise localization ability and constructing energy-efficient transmitters (TX) by using impulse-radio (IR) technology. Implementations of high-performance wireless-powered IR-UWB TXs become possible even in standard CMOS processes. Pulse generator (PG) is usually the most energy-demanding component in such wireless systems. Large energy dissipation will reduce the TX sensitivity and increase the difficulty of power management circuits design. In most wireless-powered IR-UWB TXs [1]–[3], the PG energy dissipation is less than 10 pJ/pulse. In addition, the PG efficiency is also important to provide reasonable emitted energy and, hence, good communication distance.

The basic idea of most published IR-UWB PGs is to use a high-frequency waveform generator (HFWG), which can be an oscillator, phase-locked loop or delay-line (DL) etc., and shape the output signal to generate the desired envelope by mainly three approaches: filtering [4], spectrum mixing [5], [6] or multi-pulse combination (MPC) [7], [8]. For the filtering approach, the HFWG output signal is coupled to and filtered by a pulse shaping filter so that the resultant signal can meet the spectrum regulations. In additional to the circuit simplicity, another advantage is that the output parasitic capacitance, which is usually the dominating one inside the PG, can be used as part of the filter and tuned-out by inductors inside the filter. In other words, the capacitive and switching losses could be reduced. However, the filtered energy may be wasted and on-chip spiral inductors are area-demanding.

The spectrum mixing approach consists of a local oscillator (LO) and a mixer like conventional narrowband TXs, the high-frequency LO output is then mixed with the envelope shape. The power consumption and area are relatively large because more components are needed compared to the other two approaches. Moreover, the leakage from LO to the antenna could be problematic. However, a definite advantage is the ability to generate high-quality bi-phase shift key (BPSK) IR-UWB signals. The mixing function could also be performed by switching the oscillator on and off (will be referred to as switching oscillator, SO, approach) [9]. This eliminates the mixer and LO leakage, but reduces control of emitted pulse shape. The SO approach is reported to be energy efficient because of its simplicity. Nevertheless the low antenna resistance loads the tank and reduces its quality factor (QF), large bias current is needed to start-up the oscillation and obtain a large output swing [9]. This makes the SO approach less suitable for wireless-powered IR-UWB radios.

MPC IR-UWB PGs usually utilize DLs as the HFWG. Based on the propagation delay (PD) of the DL and output drivers with different strength, Gaussian-approximate waveforms can be obtained. The MPC approach is shown to be very energy-efficient (5.2 pJ/pulse has been reported in [7]) and small-size because it contains mainly digital gates. Nevertheless most of the MPC IR-UWB PGs operate at the low UWB band, this is because the capacitive and switching losses due to the output parasitic capacitance increase with frequency. Also, it is not easy to control the envelope accurately due to process variations, filtering and/or calibration may be required.

A low-power DL-based MPC on-off-keying (OOK) IR-UWB PG is presented in this paper. It uses an on-chip spiral inductor to tune out the output parasitic capacitance, the driving requirement and, hence, the transistor size of the output drivers are reduced. In other words, the capacitive and switching losses are also reduced which makes the proposed PG energy-efficient. Moreover, the center frequency (f_C), output power and pulse-width (PW) are adjustable depending on channel conditions and data rates. A similar structure has been adopted in [1], however limited analysis and results have been presented. The proposed PG is realized in a TSMC 90 nm CMOS process and shows good measurement results.

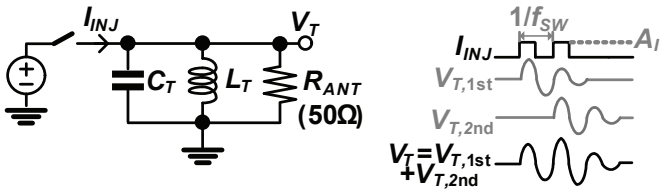

Fig. 1. (a) Proposed system of the PG and (b) its timing waveforms.

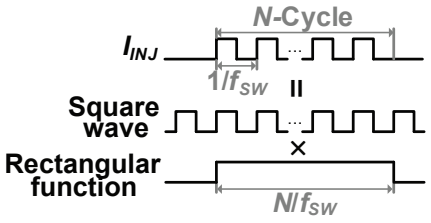

Fig. 2. Timining waveforms related to I_{INJ}.

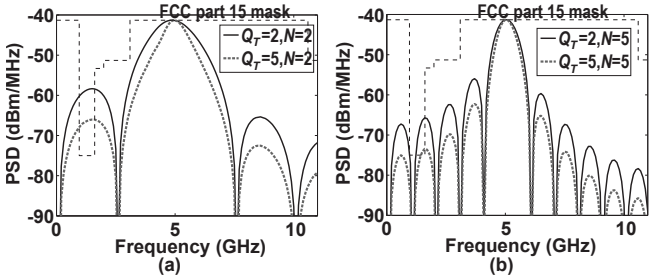

Fig. 3. System-level simulated PSD with different Q_T. (a) N=2 and (b) N=5.

II. IR-UWB Signal Generation

The basic idea of the proposed PG is to inject energy into an RLC tank which consists of the antenna resistance (R_{ANT}) periodically as shown in Fig. 1a. The tank resonant frequency (f_o) and quality factor (Q_T) are given as:

$$f_o = \frac{1}{2\pi\sqrt{L_T C_T}} \tag{1}$$

$$Q_T = \frac{R_{ANT}}{\omega_o L_T} = \omega_o C_T R_{ANT} \tag{2}$$

Assume N energy pulses with 50% duty-cycle are injected to the tank by turning on and off the switch periodically with a frequency of f_{SW}, every single injected energy pulse circulates back and forth inside the tank with f_o. Due to the R_{ANT}, the i-th resonanting pulse decays as:

$$V_{R,\text{i-th}} = V_P \exp\left(-\frac{f_o}{Q_T}t\right)\sin\left(2\pi f_o t\right) \tag{3}$$

The signal dies out in approximately Q_T cycle. If f_{SW} and f_o are the same, the resonanting pulses will be in-phase and added together. As a result, a higher-energy and longer-PW IR-UWB signal can be obtained. An example with Q_T=2 and N=2 is shown in Fig. 1b.

It is difficult to determine the output signal amplitude because of the system nonlinearities. Nevertheless it is important to estimate the system frequency response so that the FCC part 15 mask requirements can be met. A qualitative frequency domain analysis is performed. The waveform of the injected current (I_{INJ}) can be modeled as a square wave with a frequency of f_{SW} multiplying with a rectangular function with a width of $\frac{N}{f_{SW}}$ as shown in Fig. 2. As a result, the resultant frequency spectrum can be expressed as

$$I_{INJ}(f) = \overbrace{\frac{4A_I}{\pi}\sum_{k=1}^{\infty}\frac{\delta(2\pi(2k-1)f_{SW})}{2k-1}}^{\text{Square wave}} * \overbrace{\frac{N}{f_{SW}}\text{sinc}\left(\frac{Nf}{f_{SW}}\right)}^{\text{Rectangular function}} \tag{4}$$

where A_I is the amplitude of the injected current. Because the higher-order components of the square wave (the first term) are always out of the UWB band (for example, if f_{SW} = 4 GHz, the higher-order components will be $\geq$ 12 GHz), only the fundamental component is considered and I_{INJ} becomes

$$I_{INJ}(f) = \frac{4N \cdot A_I}{\pi f_{SW}}\left[\delta(2\pi f_{SW}) * \text{sinc}\left(\frac{Nf}{f_{SW}}\right)\right] \tag{5}$$

Its bandwidth (BW) is determined by the sinc function and the –10-dB BW ($BW_{-10\text{dB}}$) of I_{INJ}^2 is found to be $\approx \frac{f_{SW}}{N}$.

I_{INJ} is then filtered by the RLC tank. One important parameter is Q_T, large Q_T provides narrower BW and reduces the sideband energy of I_{INJ}. Nevertheless the in-band energy may also be filtered-out and the energy efficiency is reduced. Also Q_T has to be much smaller than the inductor QF (Q_L) so as to prevent insertion losses (IL) which is given as

$$\text{IL} = \frac{1}{1+\frac{Q_T}{Q_L}} \tag{6}$$

The QF of on-chip spiral inductors is normally around 10–20. Because the energy efficiency is of the most important in this work and the low-frequency (LF) sideband can be filtered-out by adding high-pass filter (HPF) or/and exploring the antenna bandpass property, small Q_T is preferred to minimize the IL. Notice that the data rate and localization ability also improve with increased BW (small Q_T) [1]. A rule of thumb is to set $BW_{-10\text{dB}}$ of I_{INJ}^2 to be smaller than or equal to the –3-dB BW of the RLC tank such that the tank provides only insignificant attenuation. In other words,

$$\frac{f_{SW}}{N} \leq \frac{f_o}{Q_T} \Rightarrow N \geq Q_T \tag{7}$$

An example is shown in Fig. 3, which shows system-level simulation results with f_o=f_{SW}=5 GHz and different combinations of Q_T and N. The peak power spectral densities (PSD) are normalized to –41.3 dBm/MHz for better comparisons. In Fig. 3a, N is set to 2. Increasing Q_T from 2 to 5 can reduce the LF sideband energy for 7.5 dB, but reduce $BW_{-10\text{dB}}$ for 32% (from 3.1 GHz to 2.1 GHz). If N is increased to 5 as shown in Fig. 3b, increasing Q_T from 2 to 5 only reduces $BW_{-10\text{dB}}$ for 14% (from 1.4 GHz to 1.2 GHz). Notice that increasing N can provide higher attenuation to the sideband energy because of the narrower BW of the sinc function, the trade-off is that the BW of the mainlobe is also reduced.

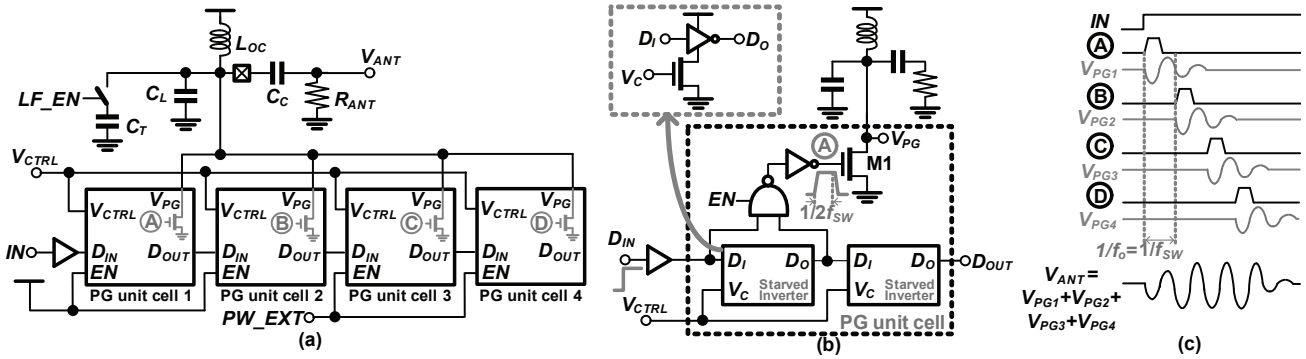

Fig. 4. (a) The proposed PG, (b) the PG unit cell and (c) the PG operation.

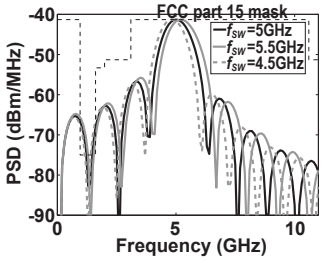

Fig. 5. Power spectra with different mismatches between f_o and f_{SW} (f_o=5 GHz).

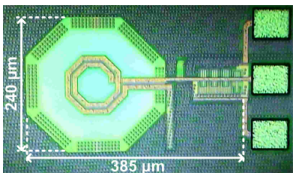

Fig. 6. A Chip microphotograph.

III. Proposed IR-UWB PG

The schematic of the proposed IR-UWB PG is shown in Fig. 4a. LF_EN='0' and PW_EXT='1' are assumed at this moment, the setting will be explained later. Instead of using a single switch driven by an oscillator as shown in Fig. 1a, several switches are cascaded and turned on and off in sequence with a frequency of approximately f_{SW} by using a DL. Energy is then injected to an RLC tank consisting of R_{ANT}, an on-chip inductor L_{OC}, a tuning capacitor (C_T) and loading and parasitic capacitors (C_L), with a small Q_T of two because of the energy efficiency consideration. The DL approach is adopted because DLs are usually simpler and more energy-efficient than oscillators.

The PG is constructed by cascading four unit cells. The schematic of unit cell is shown in Fig. 4b. The PD (with a length of approximately $\frac{1}{2f_{SW}}$) of a starved inverter is used to generate an impulse with a width of approximately $\frac{1}{2f_{SW}}$ at node A and M1 is turned on. This pulls down the output voltage and injects energy into the tank. Due to the R_{ANT}, the signal decays as indicated from (3). If f_{SW} is approximately equal to f_o by setting the control voltage of the starved inverter (V_C), the output signals from all unit cells are in phase and added together. As a result, a higher-energy and longer-PW UWB pulse can be generated. The idea is depicted in Fig. 4c. Note that the waveforms V_{PGi} (V_{PG1}–V_{PG4}, which are highlighted in grey color) represent the output signals contributed by the i-th unit cell, they are shown for illustration purposes and do not exist actually in the system.

One drawback of DL-based MPC PG is that f_C and BW are sensitive to the PD variation of the DL. The proposed PG is relatively less sensitive to this variation because the tank bandpass property concentrates the output energy at f_o. Fig. 5 shows the system-level simulated power spectra with ±5% mismatches between f_{SW} and f_o. Around ±3% variation on f_C and ±4% variation on $BW_{-10\text{dB}}$ are observed. Larger Q_T can make the PG less sensitive to the PD variation, with trade-offs as aforementioned.

The output parasitic capacitance which is usually dominating inside the system is tuned out by L_{OC}, the driving requirement and, hence, the transistors size of the output driver are reduced. In other words, the capacitive and switching losses are also reduced which makes the designed PG energy-efficient. L_{OC} connects the PG output to the positive supply rail at DC which provides electrostatic discharge protection.

Another advantage of the proposed PG is its high flexibility. The PW is scalable by adding more unit cells. If more unit cells are cascaded in series, smaller BW and higher-energy outputs can be generated. In addition, the output energy, f_C and $BW_{-10\text{dB}}$ (hence also PW) can be adjusted depending on channel conditions. If the radios nearby are using similar operating frequency, f_C can be reduced by decreasing V_{CTRL} and setting LF_EN to '1' to connect C_T. More frequency steps can be obtained by replacing C_T with a switched-capacitor array. If the interference from other radios becomes less significant, some unit cells can be disabled by setting their EN input to '0'. The energy consumption can then be reduced. In the designed PG, either two or four unit cells are enabled by switching PW_EXT.

IV. Experimental Results

A proof-of-concept prototype is implemented in a TSMC 90 nm CMOS process. A chip microphotograph is shown in Fig. 6. The core area excluding pads is 0.092 mm^2. The

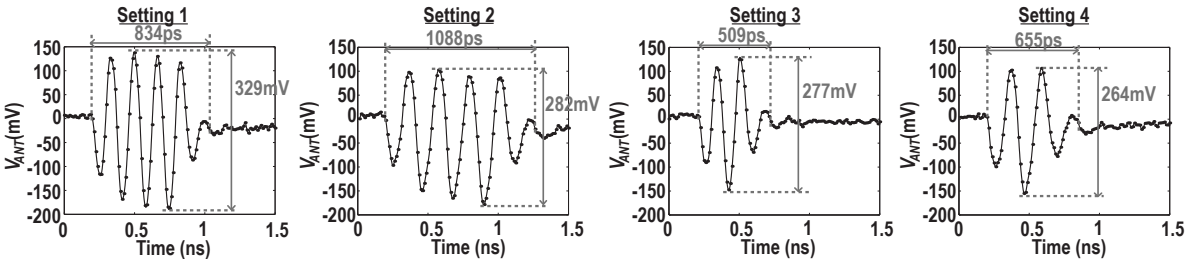

Fig. 7. Timining waveforms of the PG output.

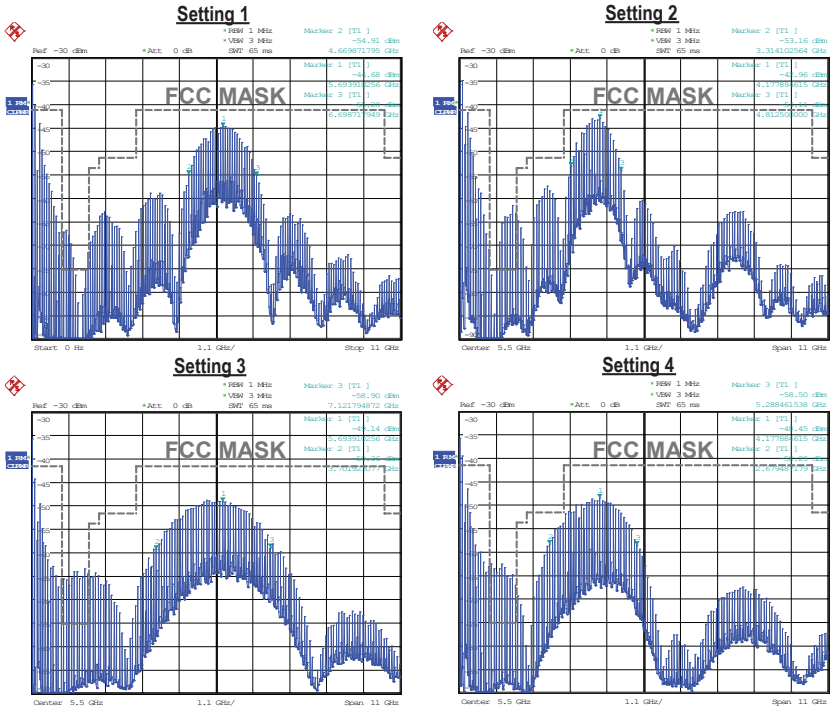

Fig. 8. Power spectra of the PG output.

supply voltage is 1.2 V. The PG output is probed on-chip and connected to a 50 Ω load. Four different settings are tested:

1) LF_EN='0' and PW_EXT='1': All unit cells are enabled (N=4) with high f_C.
2) LF_EN='1' and PW_EXT='1': All unit cells are enabled (N=4) with low f_C.
3) LF_EN='0' and PW_EXT='0': Two unit cells are enabled (N=2) with high f_C.
4) LF_EN='1' and PW_EXT='0': Two unit cells are enabled (N=2) with low f_C.

V_{CTRL} is changed accordingly when LF_EN='1'. The resultant timing waveforms and power spectra with 80 MHz pulse repetition rate (PRF) are shown in Fig. 7 and Fig. 8 respectively. f_C can be adjusted from 4 GHz to 5.6 GHz, a larger peak energy and a narrower BW can be achieved by adding more unit cells (i.e. larger N). The LF components (<900 MHz) are due to the ringing caused by the bondwires of the voltage supplies, these components can be removed by adding decoupling capacitors. The proposed PG achieves a LF sidelobe (<2 GHz) energy reduction of 15–20 dB. Some LF sidelobes violate the FCC part 15 mask at such high PRF, we assume they will be removed by adding HPF or simply exploring the antenna bandpass property.

The PG performance is summarized and compared with other published state-of-the-art IR-UWB PGs in Table I. The PG energy efficiency is commonly used to compare different PG performance [9], [10] and given as:

$$\eta = \frac{\frac{V_{P\text{-}P}^2}{8R_L} PW}{E_C} \tag{8}$$

where $V_{P\text{-}P}$ is the peak-to-peak voltage, R_L is the load resistance and E_C is the energy consumption per pulse. Nevertheless it is difficult to define the PW precisely because of the ringing caused by the bondwires. Also, eq. (8) assumes the PG output is a sinewave burst and ignores the pulse shape. To improve this, a new figure-of-merit (FoM) is proposed and given as

$$\text{FoM} = \frac{\frac{V_{P\text{-}P}^2}{8R_L} \cdot \frac{1}{BW_{-10\text{dB}}}}{E_C} \tag{9}$$

Modern spectrum analyzers can measure signal BWs precisely and $BW_{-10\text{dB}}$ can partly represents the pulse shape, hence a

TABLE I
A SUMMARY OF THE PROPOSED IR-UWB PG PERFORMANCE AND A COMPARISON WITH OTHER PUBLISHED IR-UWB PGS

	[9]	[10]	[7]	[4]	[3]	[8]	[5]	This work			
								Setting 1	2	3	4
Technology	180 nm CMOS	2 μm HBT	90 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS	90 nm CMOS			
Modulation	OOK	OOK	OOK	OOK	OOK	OOK	BPSK	OOK			
E_C (pJ/pulse)	118	790	5.2	28	9.2	20	51.5	5.2	7.5	2.8	4
$V_{P\text{-}P}$ (V)	4.9[a]	6.2	0.41	0.67	0.22	0.26	0.19	0.33	0.28	0.28	0.26
PW (ns)	1	≈1[b]	0.96	0.5	0.7	1	0.5	0.83	1.1	0.51	0.66
$BW_{-10\text{-}dB}$ (GHz)	2	1.8	1.9	4	≈3.2[b]	2	≈3.8[b]	2	1.5	3.4	2.6
f_C (GHz)	4.3	4.1	4	8	≈3.9[b]	4	≈8.3[b]	5.6	4.1	5.4	4
η (%)	25.4	10.4	7.9	2	1	0.1	0.01	4.3	2.9	3.5	2.9
FoM (%)	12.7	6.8	4.3	1	0.4	0.4	0.05	2.6	1.7	2.1	1.6
Area (mm^2)	0.19	1	0.0015	0.11	N/A	0.08	N/A	0.09			

[a] Differential output with a 100 Ω load. [b] Estimated from the figures.

more precise comparison can be made.

The proposed PG is one of the few candidates that can achieve E_C of smaller than 10 pJ/pulse. Competitive FoM and η are measured, FoM ranges from 1.6% to 2.6% and η ranges from 2.9% to 4.3%. In [7], a DL-based MPC PG with E_C=5.2 pJ/pulse and FoM=4.3% has been reported. Nevertheless it is relatively more sensitive to the PD variation of the DL as aforementioned. A BPSK PG using spectrum mixing approach has been reported in [5]. The BPSK modulations may improve the system performance, however, a very low FoM of 0.05% has been reported because the PG structure is similiar to conventional narrowband TXs.

In [9], a SO topology with a very high FoM of 12.7% has been demonstrated. However, the measured E_C is 118 pJ/pulse, we assume the large E_C is due to the fact that large current (peak current of 70 mA) is needed to start-up the low-QF LC oscillator and maximize the output swing (and hence η). In [10], an impulse-forming approach has been proposed and a FoM of 6.8% has been reported. The idea is similar to distributing amplifier, an impulse is inputted to an off-chip tapped DL network which consists of transmission lines and bondwire inductors. The impulse and its replicas are then delayed, scaled and combined at the PG output. The large FoM is because of the usage of HBT transistors which provides higher power capacity and high speed. However, this PG is not suitable for wireless-powered IR-UWB radios because of its large E_C of 790 pJ/pulse and large area due to the pad and bondwire inductors. Also, the HBT process fabrication is more expensive compared to the CMOS counterparts.

V. CONCLUSION

A low-power energy-efficient OOK IR-UWB PG intended for wireless-powered IR-UWB radio applications has been presented. The output power, f_C and PW are controllable depending on channel conditions and data rates. Qualitative frequency-domain and transient analyses have been presented and matched with the measurement results. A new FoM has been proposed to compare different PGs in a more precise way. A proof-of-concept prototype has been successfully implemented in a TSMC 90 nm CMOS process. The core area is 0.092 mm^2. Measurements show the energy consumption and FoM to be 2.8–7.5 pJ/pulse and 1.6–2.6% respectively, which is competitive to most published IR-UWB PGs and proves the proposed PG suitable for wireless-powered radios. The output swing is 277–329 $mV_{p\text{-}p}$. PW and f_C ranges 509–1088 ps and 4–5.6 GHz respectively, which provides freedoms to optimize the system performance.

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